



## Additional Meetings

### SystemC Technology Symposium

Monday, July 24 • 12:00 pm - 1:30 pm

Rm: 200-212

The Open SystemC Initiative (OSCI) invites you to learn how recent advancements in SystemC apply to you today and moving forward:

Hear from industry experts on recent SystemC advancements and using SystemC for doing real world system-level design. Status updates on the technology roadmap, IEEE 1666 and TLM will be presented. (complimentary lunch provided)

### ACM/SIGDA Symposia/Workshop Leaders Luncheon

Monday, July 24 • 12:00 pm - 2:00 pm

Rm: 124

Organizers of symposia and workshops sponsored by ACM/SIGDA, as well as ACM/SIGDA volunteers are invited to a lunch get-together. ACM staff and SIGDA Board Members will be available for detailing and explaining the steps of starting or organizing an event. A brief overview of other new ACM/SIGDA activities will be presented.

### How Many Engineers Does It Take? The Real Issues in IP Integration

Monday, July 24 • 12:30 pm - 2:00 pm

Rm: 111

Free lunch panel. IP integration and verification is only getting more complex, expensive and risky. IP suppliers, integrators, EDA vendors, and foundries must work together in a streamlined fashion to ensure IP success. But are they? Varying degrees of IP quality coupled with a host of business and technical issues makes IP integration the key challenge in modern SoCs. Don't be left holding the cards with your next chip design. This panel will expose the interrelated and often opposing technical and business issues surrounding IP integration and explore how this fragmented industry can work together.

### NASCUG Meeting

Monday, July 24 • 2:00 pm - 6:00 pm

Rm: 200-212

You are invited to the 5th North American SystemC Users Meeting (NASCUG):

Open to DAC attendees, the focus of the NASCUG meeting is on SystemC real-world design methodologies and user experiences. Topics include techniques for integrating SystemC into the design flow and SystemC tool flows and methodologies. (reception starts at 5:00 pm)

### CEDA Distinguished Speaker Reception

Monday, July 24 • 5:30 pm - 7:30 pm

Rm: 124

CEDA Distinguished Speaker Series, beer/wine/cheese, followed by the TCAD Donald O. Pederson Best Paper Award winner entitled, *Embedded Deterministic Test* by **J. Rajski, J. Tyszer, M. Kassab, N. Mukherjee**

### Si2 Members Meeting

Monday, July 24 • 6:00 pm - 7:30 pm

Rm: 111

The annual Silicon Integration Initiative (Si2) Members Meeting will provide an overview and status report on Si2 projects, such as the OpenAccess Coalition, the Open Modeling Coalition, the Design-to-Manufacturing Coalition, the Design Technology Council, the Liberty TAB, and the LEF/DEF Governing Board. The newly-elected Si2 Board of Directors will be introduced, and industry trends are explored. Companies considering joining Si2 are welcome to attend. Refreshments and snacks will be served before and after the meeting. Please contact Bill Bayer (wbayer@si2.org) if you would like to attend.

### The SPIRIT Consortium General Meeting

Monday, July 24 • 6:00 pm - 8:00 pm

Rm: San Francisco Marriott Hotel

At DAC 2006, The SPIRIT Consortium will provide a major opportunity to hear about The Consortium's specifications and see them applied in practice by multiple users and vendors. Please join us to hear presentations on the released specifications, The Consortium roadmap and proposed IEEE 1685 standard, and see in-use demonstrations of the specifications. Enjoy a brief repast and cocktail hour on behalf of The SPIRIT Consortium! You may register your interest to attend this general meeting by emailing [info@spiritconsortium.org](mailto:info@spiritconsortium.org).

### Synopsys/Sun University Reception

Monday, July 24 • 6:30 pm - 8:30 pm

Rm: 228/230

University professors and students are invited to join Synopsys and Sun Microsystems for an evening reception including drinks and hors d'oeuvres. Prize drawings will be held throughout the evening and the following keynote presentations will be featured.

*The Future is BDA*, Dr. Richard Newton, Dean of Engineering, Univ. of California, Berkeley

*Design For Testability: The Path to Deep Submicron*, Tom W. Williams, Synopsys Fellow

Not sure what BDA is? Join us to find out.



*The 43rd Design Automation Conference • July 24 - 28, 2006 • San Francisco, CA*

## **Additional Meetings**

### **Industry Standard IP Protection System for EDA Tool Flows**

**Tuesday, July 25 • 7:30 am - 9:15 am**

**Rm: 302**

IP Vendors require security; Chip Designers require interoperability across many tools. Can one methodology satisfy both? This panel will discuss a methodology and its underlying technology that achieves these goals. Panelists from IC vendors, EDA companies, and IP providers will discuss their unique requirements and concerns and will highlight the flexibility and security necessary for an industry standard methodology to emerge. Key panel topics:

- The underlying technology
- IP provider control for the level to which their IP is visible to EDA tools and users
- Advantages of using a non-proprietary encryption mechanism
- EDA vendor requirements

### **SPICE and FastSPICE: The Next 25 Years**

#### **Synopsys Analog Mixed Signal Breakfast Event**

**Tuesday, July 25 • 7:30 am - 10:00 am**

**Rm: Marriott: Golden Gate Hall Salon B1**

Synopsys invites you to attend Synopsys' Analog Mixed Signal breakfast program on the future of SPICE and FastSPICE. HSPICE is celebrating its 25 year anniversary. Come and hear what the industry experts predict the next 25 years have in store for SPICE and FastSPICE challenges. For more information and to register visit: [http://www.synopsys.com/ams\\_breakfast](http://www.synopsys.com/ams_breakfast)

### **Brion Technology Lunch Seminar**

**Tuesday, July 25 • 11:30 am - 2:00 pm**

**Rm: 111**

Two levers that are improving the resolution and manufacturability of ultra sub wavelength patterns: one is immersion, the other is improving patterning by computational lithography. Computational lithography is used to apply and verify pattern proximity corrections and sub-resolution assist features to full-chip layouts - processes such as SRAF placement, model-based RET/OPC and model-based RET/OPC verification. Re-mapping the problem into an image-based approach allows the application of repetitive grid-based calculations to be hard coded in dedicated computing boards. The combination of the image-based approach and high speed dedicated computing hardware is revolutionizing all aspects of model-based RET/OPC.

### **SIGDA Ph. D. Forum/Member Meeting**

**Tuesday, July 25 • 6:30 pm - 8:00 pm**

**Rm: 310**

SIGDA invites you to attend our annual PhD Forum and Member Meeting. SIGDA members are invited, as we are all members of the EDA Community. We will begin with a presentation of SIGDA's programs and this year's SIGDA Technical Leadership Awards, but the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives students feedback on their research, and gives the EDA community a preview of work in process. Also, light refreshments will be served at 7:30 pm. For more information, see <http://www.sigda.org/daforum>.



## Additional Meetings

### Escape from Analog Alcatraz through OpenAccess Synopsys Interoperability Breakfast Event

Wednesday, July 26 • 7:30 am - 9:30 am

Rm: 302

Chi-Foon Chan, President/COO of Synopsys, invites you to attend Synopsys' interoperability breakfast. Speakers including Philippe Magarshack, Front-End Technology and Manufacturing Group VP and GM of Central CAD and Design Solutions at STMicroelectronics, and Jim Hogan, Industry Veteran, discuss the benefits and challenges of enabling interoperability for analog and custom design through OpenAccess. Find out who wins the annual Tenzing Norgay Interoperability Achievement Award. For more information and to register, visit [www.synopsys.com/interop/breakfast](http://www.synopsys.com/interop/breakfast)

### Lessons from the Trenches Real-World ESL Project Experiences - Are the Advantages Worth the Cost and Effort?

Wednesday, July 26 • 12:00 pm - 2:00 pm

Rm: 228 & 230

A panel of users and tools vendors will discuss real world examples of how electronic system level design tools and methodologies are being used today to improve quality, reduce risk and improve time-to-market. Issues to be addressed:

- The usability of the current generation of ELS tools
  - The amount of training/support required to achieve productivity with ESL point tools
  - What it takes to put together and support a cost effective ESL flow
  - What are the quantifiable benefits of the ESL flow
  - What has worked/what has not
  - Next steps in ESL for each panel member's company
- For more information or to register contact [r.monge@vastsystems.com](mailto:r.monge@vastsystems.com)

### ACM TODAES Editorial Board Meeting

Wednesday, July 26 • 12:00 pm - 2:00 pm

Rm: 112

Annual Editorial Board meeting of the ACM Transactions on Design Automation of Electronic Systems (ACM TODAES).

### Fourth Annual Hacks and Flacks Roundtable Discussion at DAC

Wednesday, July 26 • 3:00 pm - 4:30 pm

Rm: 302

Hours, days and weeks are spent strategizing and agonizing over public relations and marketing plans. Once plans are finalized, a large amount of money is invested on implementation. Time, effort and company dollars are spent with the goal of reaching "key" customers and gaining the attention of various audiences. BUT...do we? Does our message reach the audience who ultimately makes or breaks the sales decisions? Where do your customers get their information? What makes a positive impression on customers for EDA and IP products? What direct effect does public relations have on sales and other corporate departments? Please join us for a lively discussion among EDA customers such as Texas Instruments, STMicroelectronics and Atheros Communications along with public relation and marketing professionals to discuss these questions and find out what they read and what media they believe most influences their purchase and investment decisions.

### CANDE Meeting

Wednesday, July 26 • 6:00 pm - 7:30 pm

Rm: 112

CANDE is a joint Technical Committee on Design Automation for the IEEE Circuits and Systems Society (CASS) and the Council on Electronic Design Automation (CEDA). It is the sponsoring committee from CASS and CEDA for both ICCAD and DAC. CANDE brings design automation professionals together to build relationships, and to sponsor a workshop and initiatives that improve the CAD/EDA industry. Please visit the CANDE website: (<http://www.cande.net/>) for more information.

### Birds-of-a-Feather (BOF) Meetings

Wednesday, July 26 • 6:30 pm - 8:00 pm

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at The Moscone Center, Wednesday, July 26, 6:30 pm - 8:00 pm. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting sign up at the Information Desk located in the lower North Lobby. A room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the Information Desk.