

DAC/ISSCC Student Design Contest Guidelines for Submission

The Student Design Contest is organized by the Design Automation Conference (DAC) and the International Solid State Circuits Conference (ISSCC) to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. The contest is sponsored by DAC, ISSCC and a number of semiconductor and EDA companies.

Criteria for Entering the Contest

Submissions are invited from full-time graduate and undergraduate students. The design work submission must have taken place as part of the students' course or research work at the university and must have been completed within 18 months prior to the submission **deadline: 5 pm MST, Wednesday, December 6, 2006.**

There are three categories for the Student Design Contest submissions: **Operational** chip design, **System** level design and **Conceptual** design.

- **Operational** chip designs have been implemented and tested. Proof of implementation in the form of die- or board-photographs and measurement data must be supplied.
- **System** level design implemented with commercial off-the-shelf ICs and programmable devices (e.g. FPGA). Proof of implementation in the form of system setup photographs and measurement data must be supplied.
- **Conceptual** designs need not have been implemented but must have been thoroughly simulated and must include a test plan.

Designs can be for analog, digital, or programmable circuits and systems. Submissions can be embodied as integrated circuits, reconfigurable processors, SoCs, platform-based or embedded systems designs. Examples include:

- Analog Integrated Circuits
- Digital Integrated Circuits
- FPGA based designs
- Reconfigurable Processors
- SoC / Platform-based designs
- Embedded Systems
- MEMS/Optics/Bio-Chips

The contest allows entries of both integrated circuits and electronic systems (board-level designs) in the following areas: Operational chip (built and tested), system level design (built and tested) and Conceptual chip (designed and simulated). Operational chip designs must have been built and tested. Proof of implementation in the form of die- or board- photographs and measurement data must be supplied. System level design must have been built and tested. Proof of implementation in the form of board-photographs and measurement data must be supplied. Conceptual chip designs should not have been implemented but must have been thoroughly simulated and must include a test plan.

The project must fall within the design areas described above. The project can originate from:

- Undergraduate Class Work
- Undergraduate Research Work
- Graduate Class Work
- Graduate Research Work

The design work must have taken place at an academic institution.

Students must submit descriptions of their designs, up to 6 written pages including the abstract and not more than 10 diagrams and figures. They will be evaluated on the following criteria:

- Motivation/Justification (Why was this done?)
- Description of the design process (How was this done?)
- Describe EDA tools and methods used (How did they facilitate the design activity?)
- Functional description of final project (How does it work?)
- Physical description, size, speed, power etc. (How well does it perform?)
- Testing strategy and results (Simulation for Conceptual category) (Did it work?)
- Future work – (how can the design/work be extended?)
- Summarizing conclusions from the work (What was learnt?)

Submitted designs must not have received awards in others contests. If the design has been accepted as a regular paper for presentation at ISSCC, a companion student design contest submission must have substantially different content. Re-submission of the same material will be rejected. The student design contest submission must describe in detail the motivation, project work undertaken, methods and CAD tools used, results and conclusions. Follow the content guidelines outlined in the next section.

Submitting a Design

Submissions must be in the DAC paper format, and must be submitted electronically via the DAC web site (www.dac.com). Submissions must include the title, a 60-word abstract, and the document describing the design, not to exceed 6 written pages including the abstract and not more than 10 diagrams and figures attached. The **deadline** for submission is 5 pm MST, Wednesday, **December 6, 2006**. Refer to the DAC web site, "Call for Papers," for additional information. *Be sure to read the sections titled "Regular Papers Due November 20, 2006" for layout and file format requirements, and "Student Design Contest Due December 6, 2006".* Unlike DAC papers being submitted for review, do list the author's name(s) and affiliation(s) on your SDC submission.

It is appropriate for a professor to be included as a co-author if he/she was instrumental in your approach to the design, or provided other guidance that contributed to the success of your design.

Writing style should be clear and concise. Remember that the judges' expertise may not be in the area of your project. Make your explanations straightforward and understandable. Design for testability is important. Discuss testing issues you have considered in the design, and approaches you took or will take in testing. Engineering specifications and performance statistics can be efficiently presented in tabular form.

You may want to address some of the following questions and issues in your written report:

System Overview

- Motivation for designing the chip or system.
- Is the implementation medium appropriate?
- Does this design satisfy the system requirements?
- What is unique about this project?
- What novel ideas or elegant solutions does the design include?

Implementation and Engineering Considerations

- Specifications: functional, timing, electrical, and environmental (temperature).
- Trade-offs: architectural and circuit trade-offs, I/O considerations, floor-planning and interconnect approaches. Emphasis should be placed on why you did what you did.
- Timing and Critical Paths. What clocking scheme is used? Why?
- Which paths are critical? Have you simulated or measured their delays?
- Block Diagram, Logic / Circuit Diagrams, and Algorithms.
- What role did design automation tools play in the implementation of your design?
- Photo or Final Layout Plot (annotate so various blocks can be identified).
- Verification/Simulation (keep it brief): how did you assure that the chip would work as specified?

Testing

- How did you, or will you, test this part with I/O pins only?
- What test equipment did you use?
- Actual test results, if available, should be summarized.

Statistics

- Die size, total power, number of transistors, density of layout, maximum clock speed, etc.

Judging

A panel of experts from industry and academia will judge the submissions. Judging criteria will include originality, soundness of engineering, technical difficulty, innovation, measured performance and testing, analysis and discussion of results, conclusions, and the quality of the written submission.

Contest Awards

Winners will receive a financial award and a design contest award certificate of achievement. Awards will be given at the Design Automation Conference in June 2007, San Diego, California.

Winners will attend ISSCC 2007 and DAC 2007 for student contest presentations. Awards winners will be notified prior to the conference and offered travel assistance to attend the conferences. Winners will be invited to a special poster session at ISSCC in February 2007.

At DAC, award winners will participate in a technical presentation session on the DAC show floor. The submissions will also be displayed as posters at DAC University Booth on the show floor. Selected winning entries may be included in the DAC technical program at the discretion of the technical program committee.