
Soft-error-rate estimation in sequential circuits utilizing a scan ATPG tool

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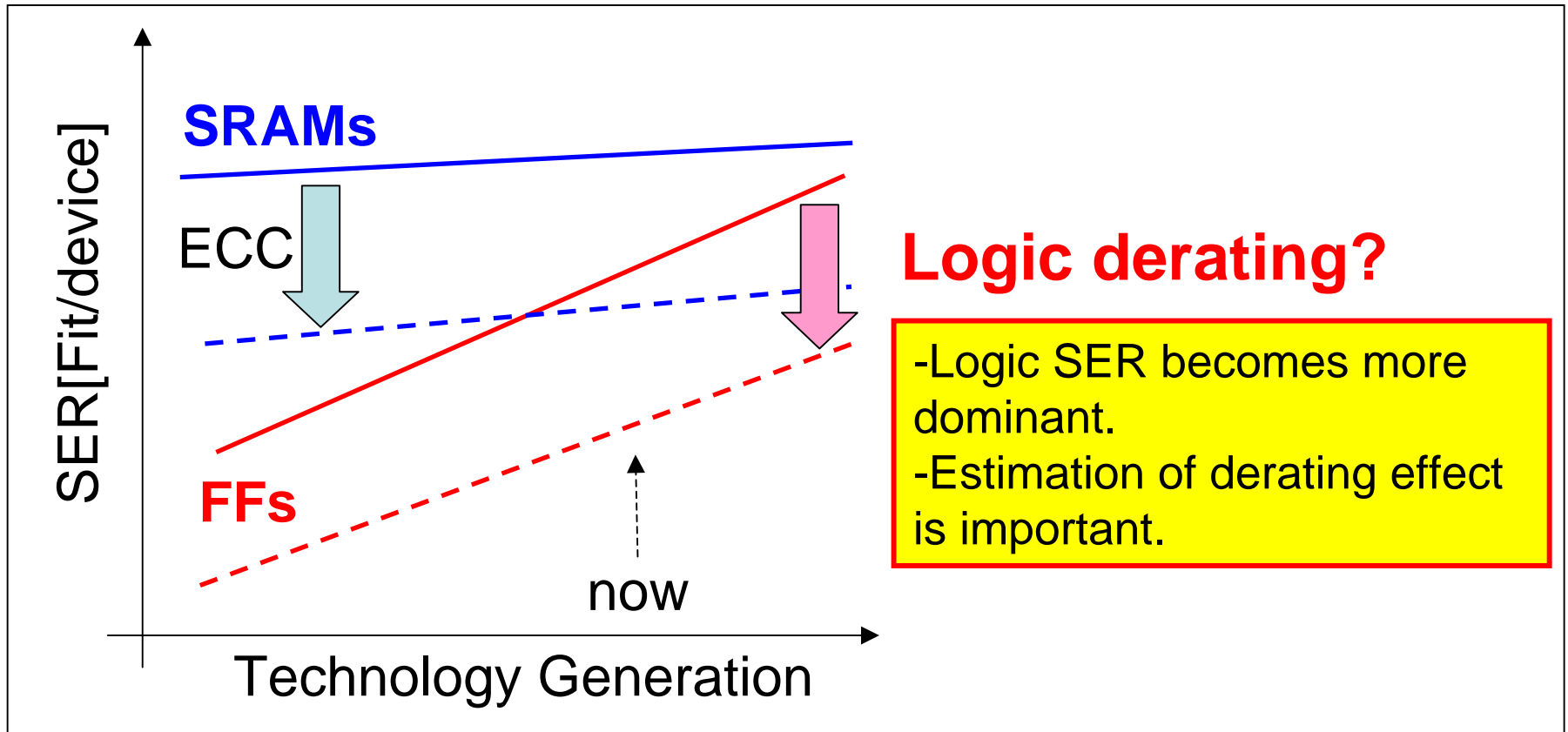
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Background

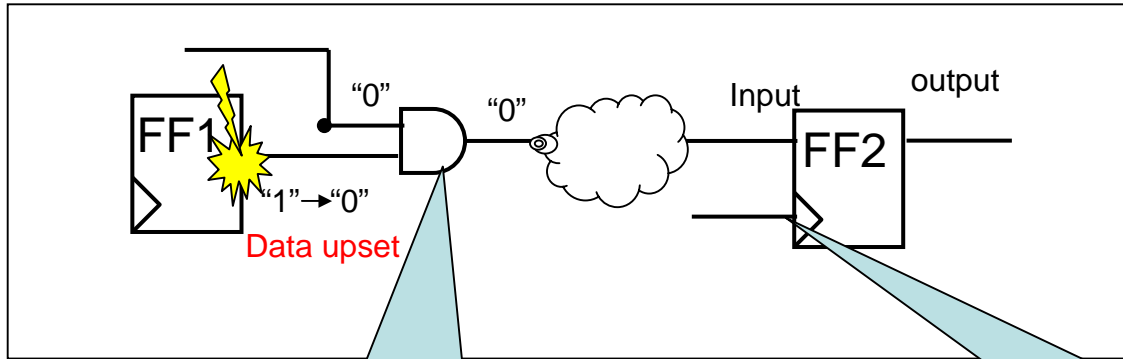
RAM-ECC in reliable products for automotive and medical use could make logic SER dominant.



Derating Factors for the SER

The following two derating factors alleviate the soft-errors in logic circuits.

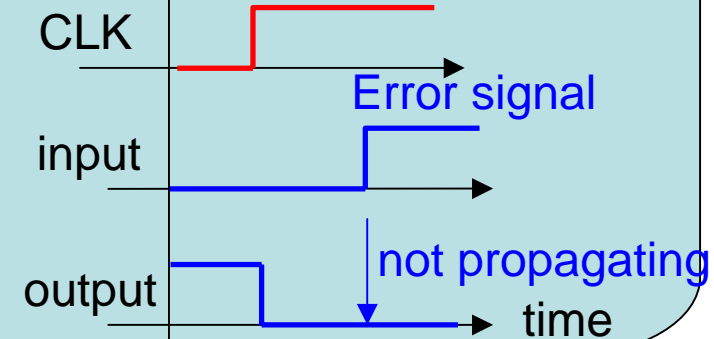
➔ Accurate estimation of derating factors is important.



This work

Logical Derating
Masking of error propagation

Timing derating

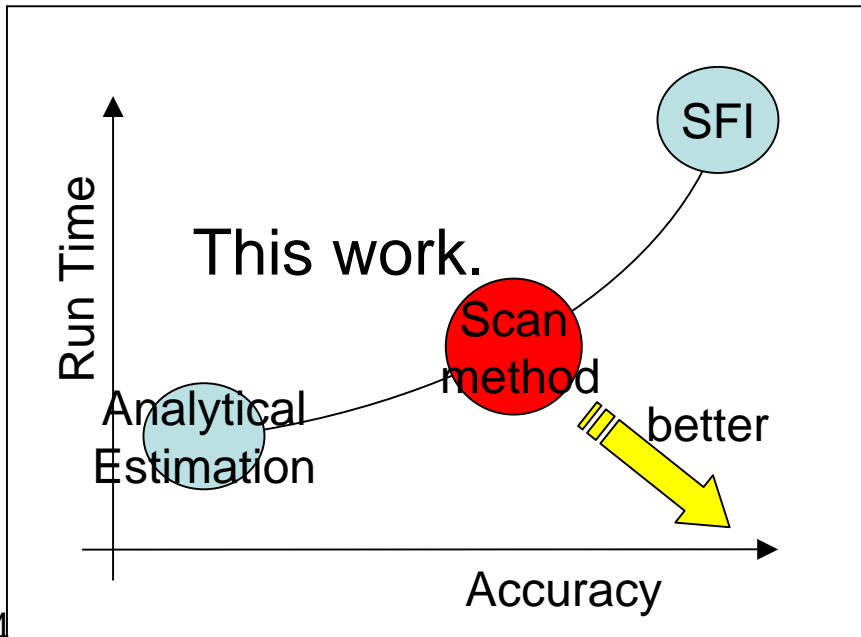


Motivation

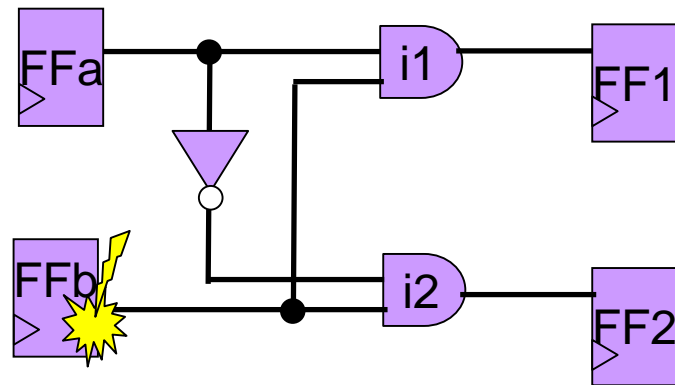
The LD estimation of general simulation method is too elaborate, consuming extensive time.

- statistical fault injection (SFI) using gate-level netlists, or using latch-accurate RTL.

➔ This work: a simple but accurate method for LD estimation using a traditional scan ATPG tool.



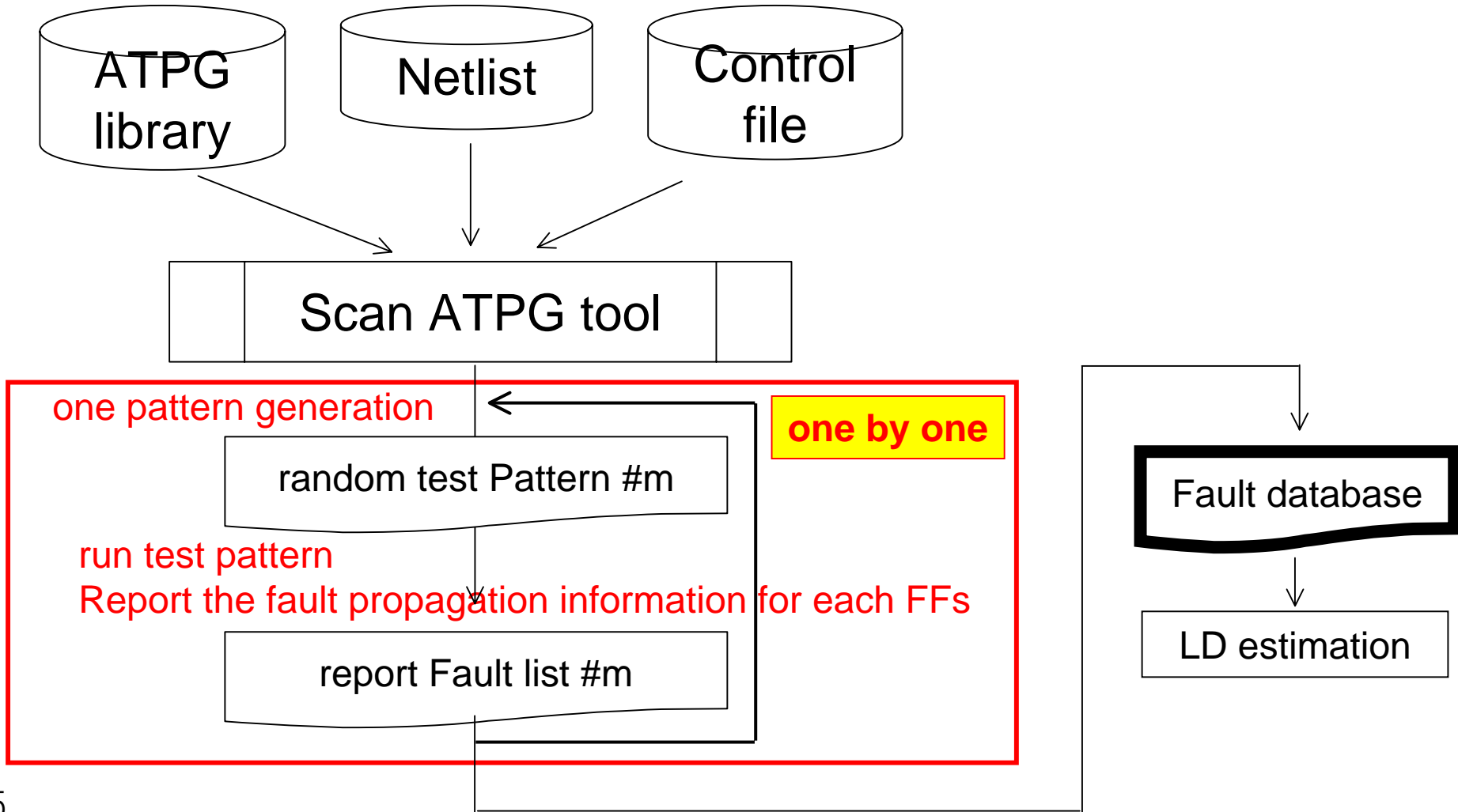
The propagation probability of AND circuit is 0.5.
The upset data of FFb always affects the FF1 or FF2.



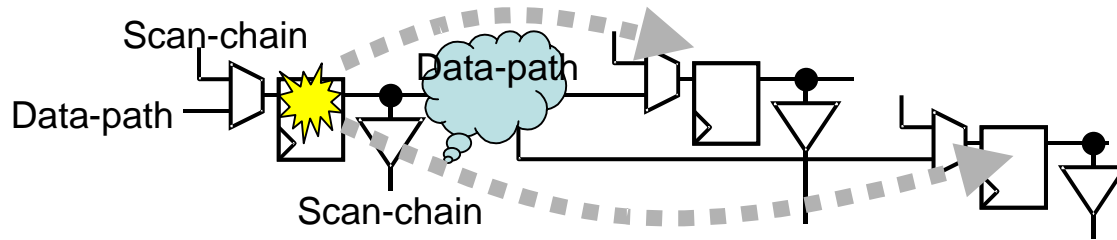
Analytical Estimation : $LD=1-(1.0-0.5)^2=0.75$
Scan method : $LD=1$

LD Estimation Methodology

It utilizes scan ATPG tool with the scan-test data in the product design flow , and thereby would not require any additional preparation nor input vectors.



LD Fault Database



V : The fault propagates to some of the next stage FFs
 blank : The fault does not propagate to any of the next stage FFs

SCAN-IN Random-pattern trial	FF number							Logic derating (LD) = "V" ratio	
	1	2	3	4	5	50582	for each trial	Cumulative for N-trial
1	V	V				V	0.254	0.254
2	V				V		0.249	0.252
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
10000	V		V			V	0.245	0.252
LD for each FF	1.00	0.05	0.01	0.13	0.85	0.25		0.252

Note: Stuck-at-0 and stuck-at-1 faults are not distinguished.

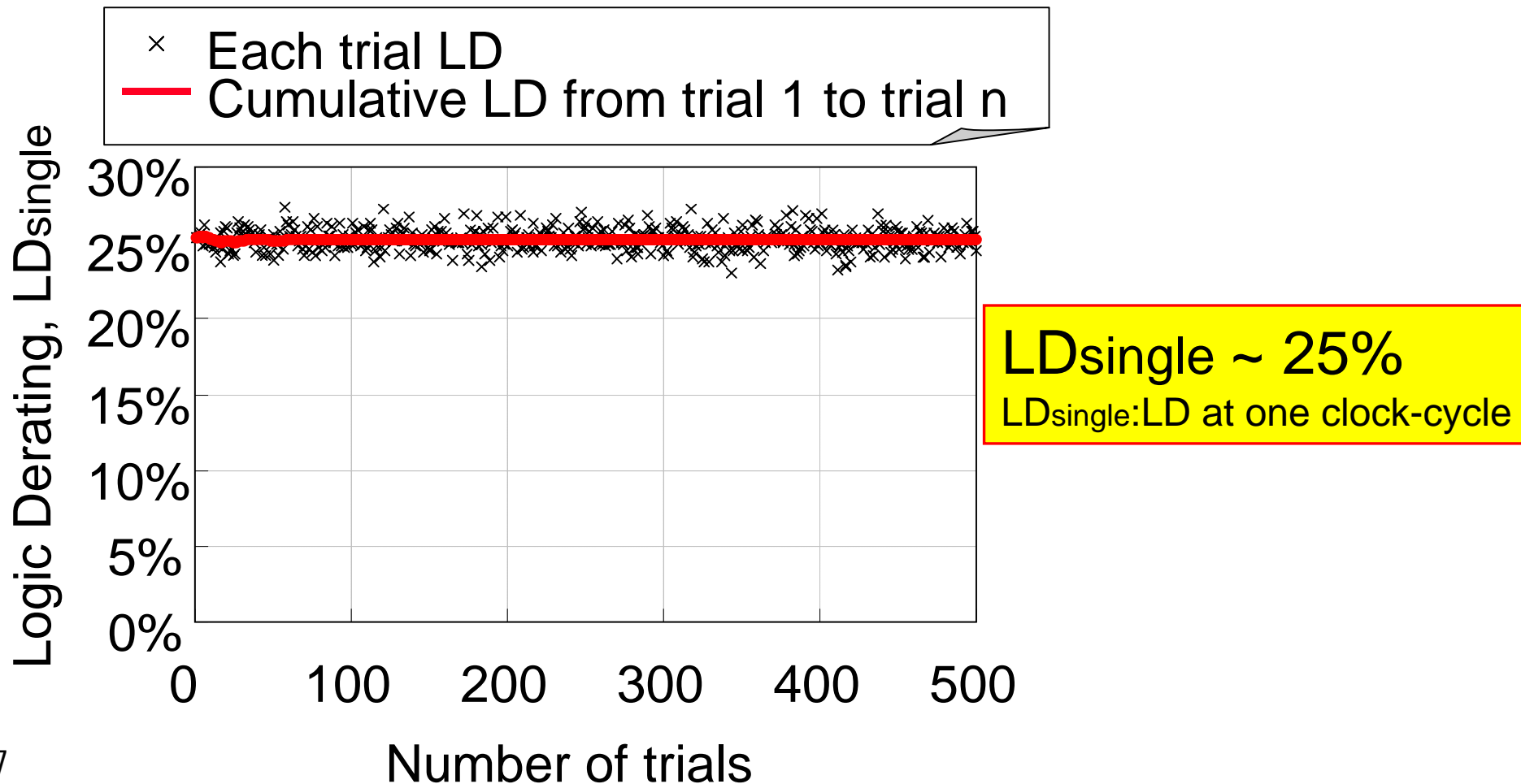
**Statistically
averaged LD**

LD Estimation Result

The LDs for each trial are in the range of 22%~28%.

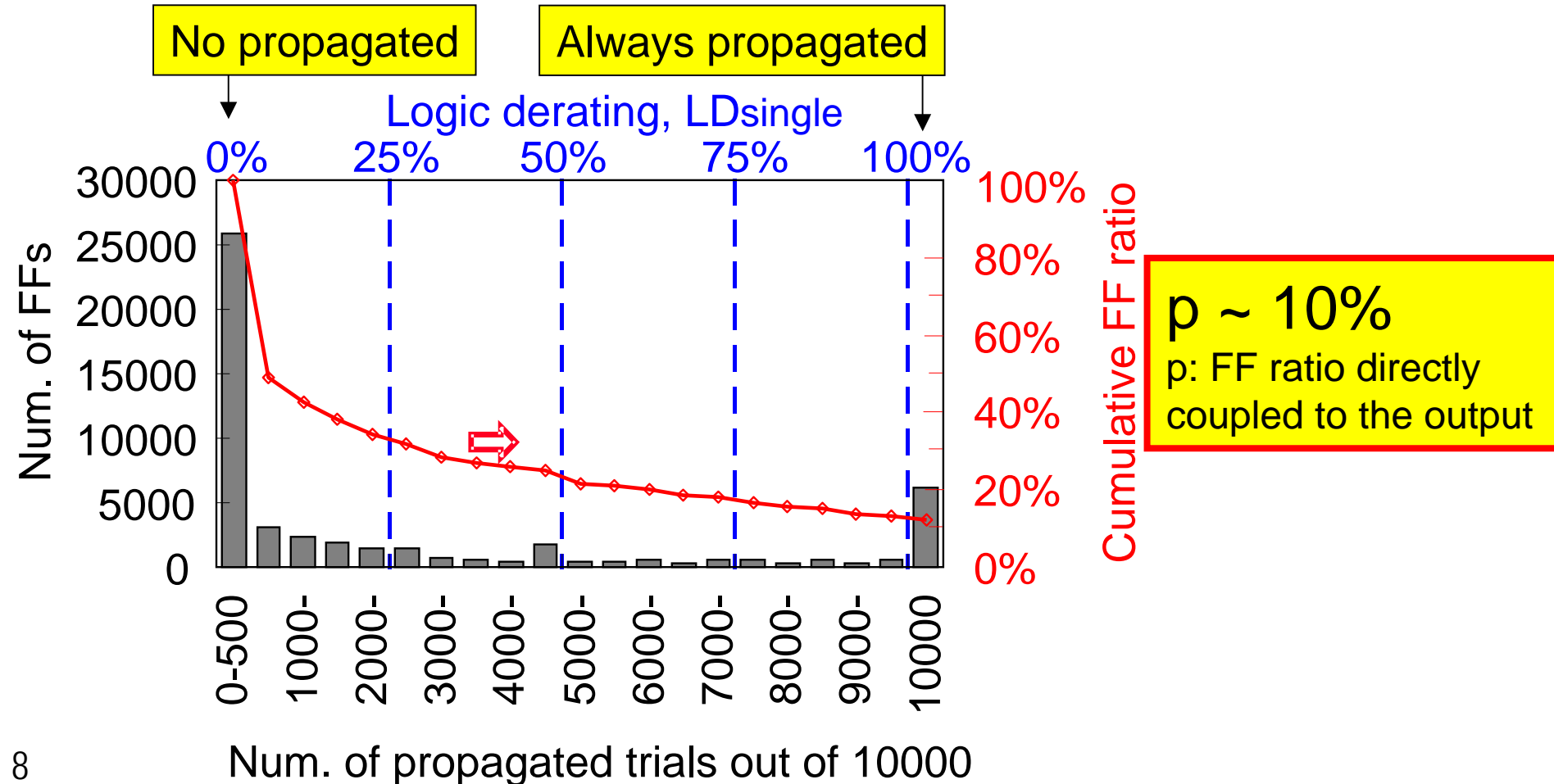
The product microcontroller with approximately 50k FF cells is used for this feasibility study.

The one trial run-time is about 4 seconds.



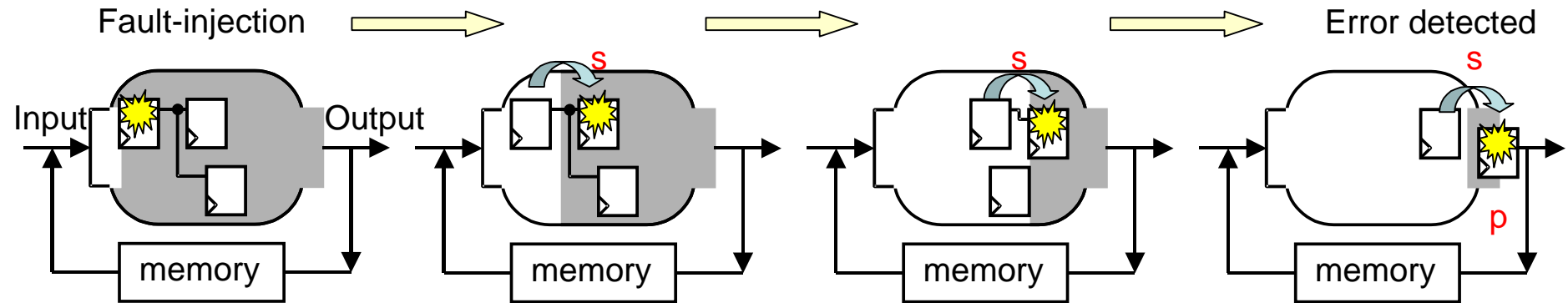
LD Distribution for 50k FF

Around 25K out of 50k FFs have the LD less than 5%.
Around 10% out of 50k FFs always propagate the injected fault to the next stage.



Chip LD Estimation

The chip LD (LD_{chip}) should be smaller than the LD at one-clock cycle (LD_{single}), because the fault reaches to the output after several clock cycles.



Num. of CLK to reach output	FF ratio (a)	Logic derating for multi-cycle (b)	contribution (a) X (b)
0	p	100%	p
1	$(1-p)/3$	s	$s * (1-p)/3$
2	$(1-p)/3$	s^2	$(s^2) * (1-p)/3$
3	$(1-p)/3$	s^3	$(s^3) * (1-p)/3$

Total LD_{chip} : $p + (s+s^2+s^3)*(1-p/3)$

p : FF ratio directly coupled to output,
 s : propagation ratio from FF to FF at one cycle

Logic Derating for Multi-Clock Cycle

The LD_{chip} can be estimated as follows.

$$LD_{chip} = p + \left(\sum_{m=1}^n s^m \right) \times (1 - p) / n$$
$$= p + \{ s \times (1 - s^n) / (1 - s) \} \times (1 - p) / n \dots (1)$$

The “p” (FF ratio directly coupled to the output) ← LD distribution results.
The “s” (propagation rate from FF to FF) ← eq. (2)
The “n” (Average clock-cycle from input to output) ← FF stage estimation

The LD_{single} is equal to that obtained from the scan method.

$$LD_{single} = p + s \times (1 - p) = 25\% \dots \dots \dots (2)$$

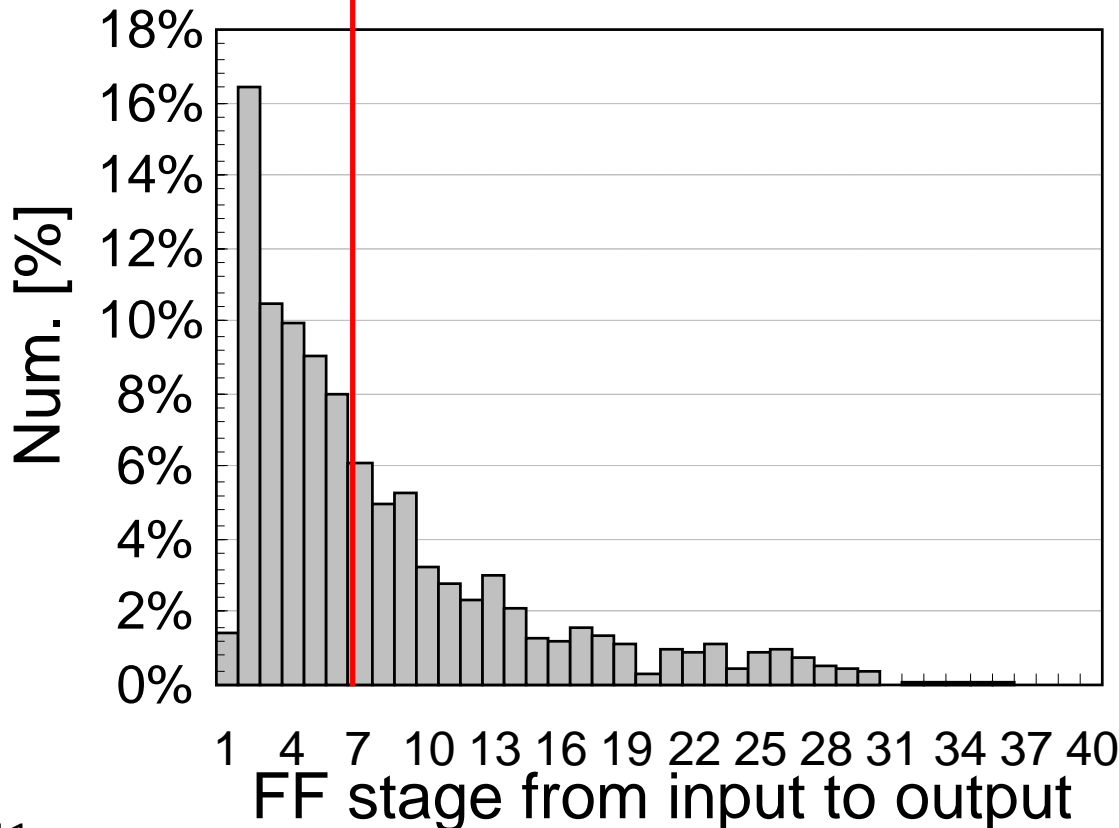
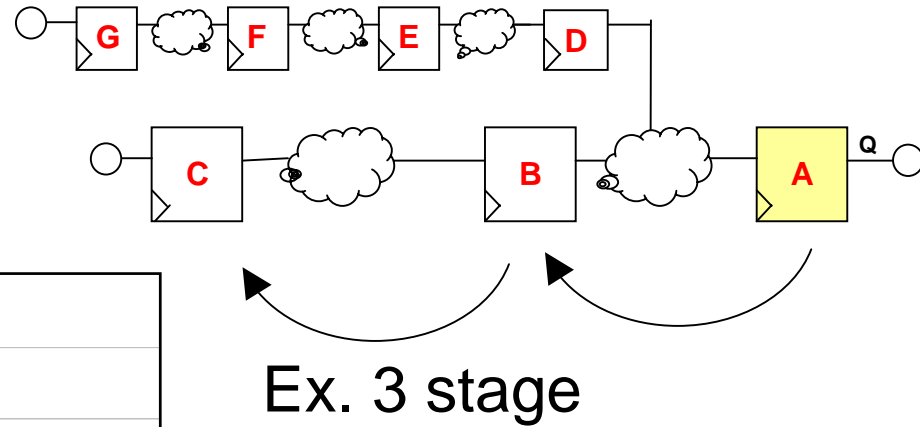
The “p” is 10% so the “s” is 17%.

s ~ 17%

Average Clock Cycle from Inputs to Output

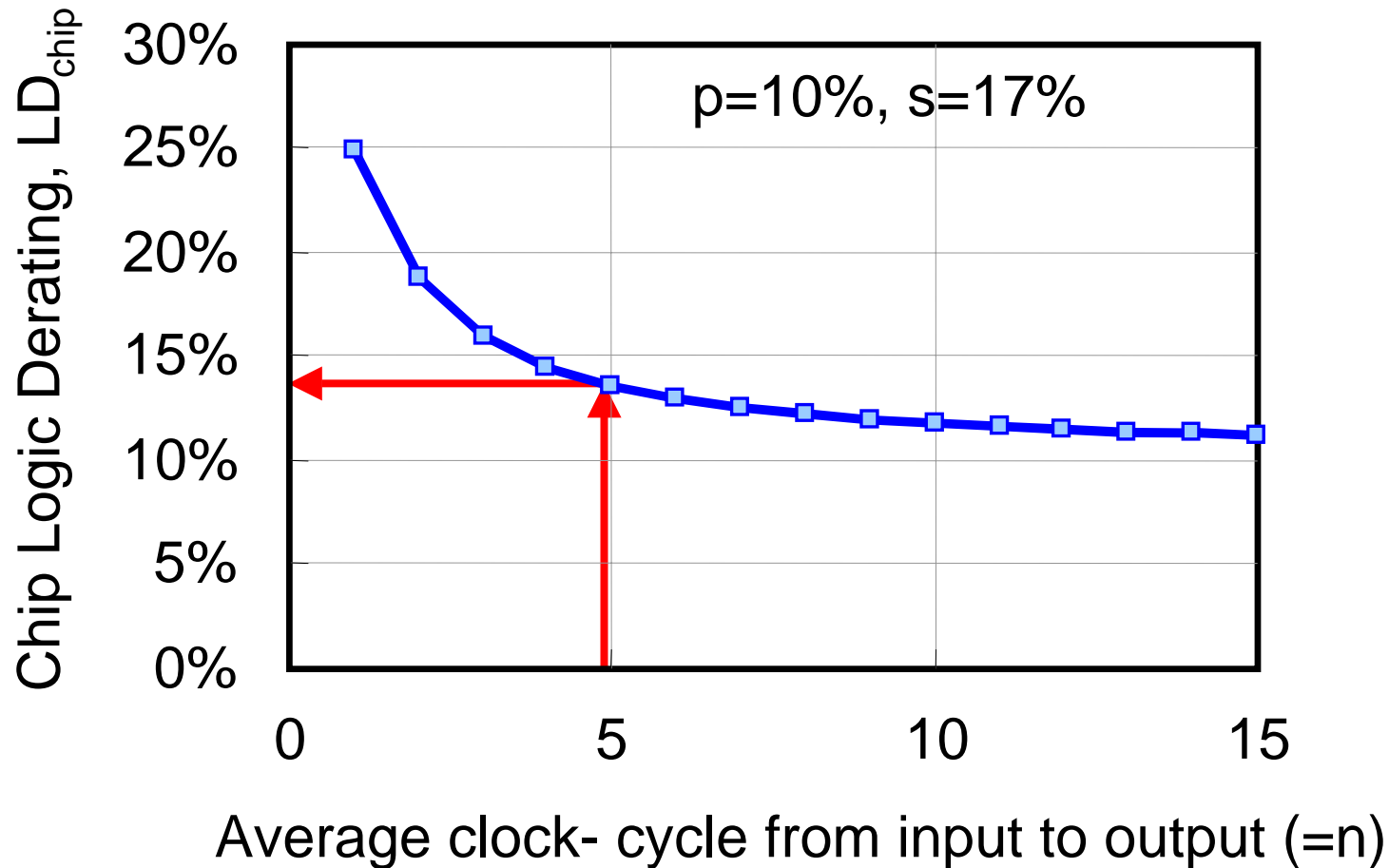
The “n” (average clock cycle from input to output) is around 5.

FF stage MEDIAN=6
→ FF-to-FF 5cycle



Logic Derating for Multi-Clock Cycle

The LDchip is estimated to be 12%~13% at $n=5$.



Summary

- The methodology for simple and accurate SER estimation in sequential circuits including the logic derating was proposed.
- It utilizes scan ATPG tool with the scan-test data in the product design flow, and thereby would not require any additional preparation nor input vectors.
- The LD_{chip} was estimated to be 12%~13% for an embedded-processor.

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