



Algorithm for Analyzing Timing Hot-Spots



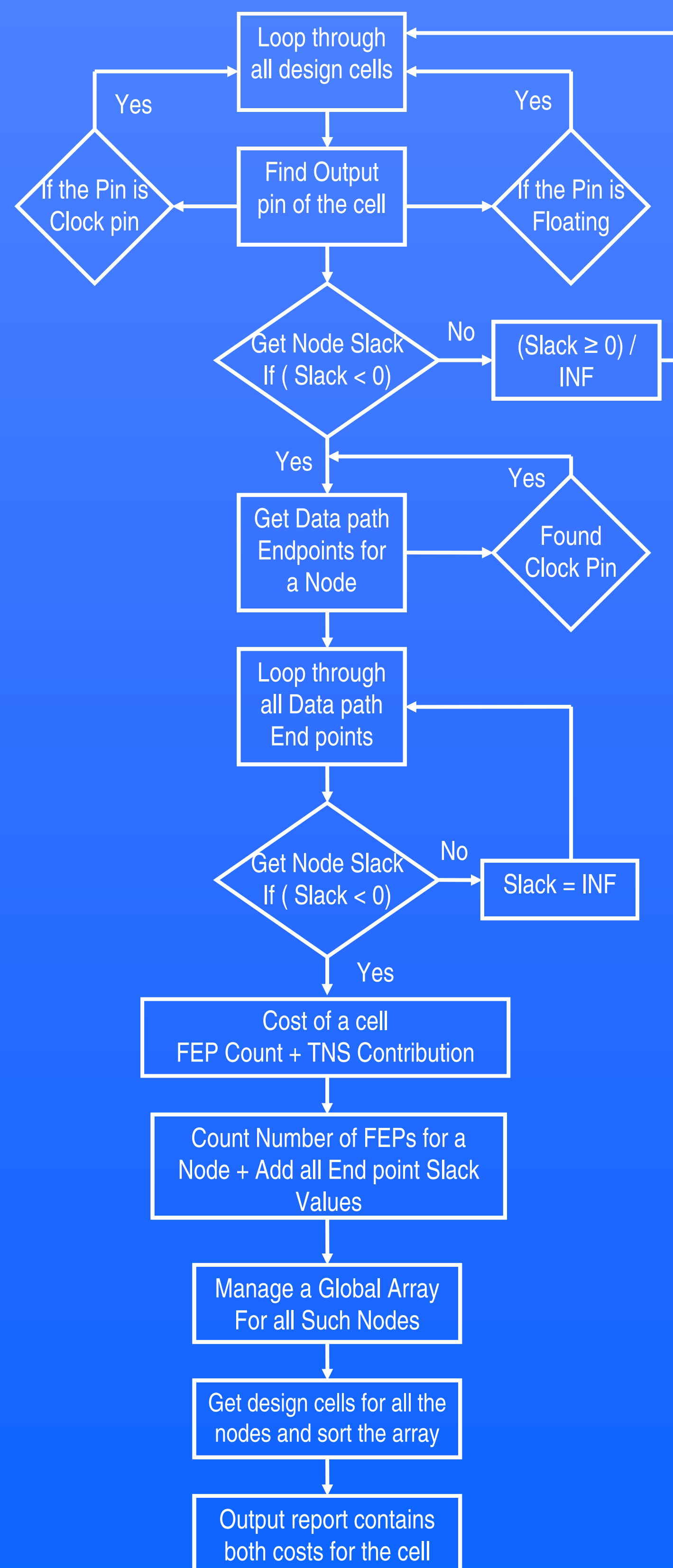
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Introduction

Achieve timing closure is a prime requirement for almost all the designs. When a design contains large number of timing violations, it is a tough task to identify a probable cause for the same. Algorithm discussed here can act as a probable solution in finding out such timing hot-spots in a design very quickly in an efficient manner.

Algorithm for Searching Timing Hot-Spots

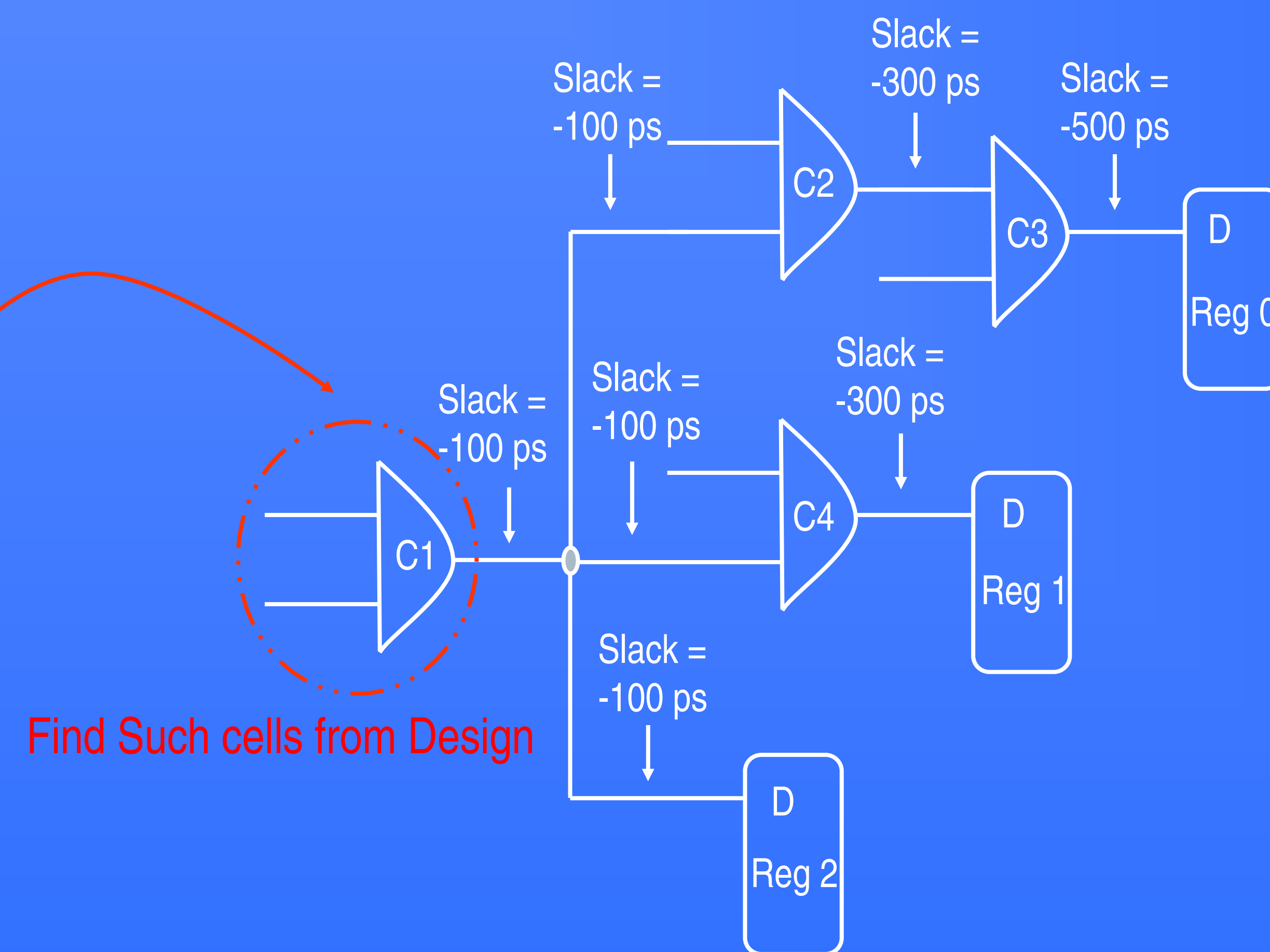
Resolving timing violations one by one require huge effort and time to converge at optimum solution. Algorithm discussed here, can save these efforts and time by reporting starting points of multiple timing violations. The cells in design not able to achieve stage delay budget assigned to them are timing hot-spots for the design. This algorithm separates out all such cells with their respective cost of failure. Prerequisites for the algorithm is timer updated design. Algorithm for finding timing hot-spots from design is as shown,



Example

This algorithm is useful for analyzing violations in both worst and best corners. Identical reports can be generated for violations in both the corner. The output report shows design cells along with their FEP count and TNS Contribution.

In the following example cell C1 is present in three failing paths. The timer is updated for the design, hence the slack values are present at each node in these paths. As shown, timings are not improved after cell C1 and went bad in each stage. The algorithm searches whole design for such cells, and sorts them in descending order keeping a cell with highest number of FEP at first in output report.



TNS (through C1) =
 $(-500\text{ps}) + (-300\text{ps}) + (-100\text{ps}) = -900\text{ps}$

If it is possible to resolve the timing issue with such one cell, a number of failing paths passing through that cell can be benefited as a result. If improvement of 100ps is possible at output of C1 than equivalent benefit in TNS would be more than 300ps.

Negative cost for a cell is a measure of the effect of that cell on timing failure. It can be reported two ways by the algorithm. One is the number of failing paths through that cell, and the other one is TNS (Total Negative Slack) contribution of that cell. Those two costs for cell C1 are,

1. Number of failing paths through cell C1 = 3
2. TNS Contribution of cell C1 = -900ps

Probable Causes

To achieve timing closure for a design containing large number of timing violations, one should look for timing-hotspots. They are the places in design most likely to benefit from any design related changes for timing closure. These nodes are the starting points for timing violations in design. Probable Causes for such situations are,

1. Selected library cell for instance is not able to meet timing budget of that stage
2. Reference cell selected from HVT/RVT library (instead of LVT library) for constrained region
3. Large Output load for the cell (fanout or length of output net)
4. Tight timing constraints defined for the region
5. Physical constraints near by the cell location

Reports

Cell	FEPs	TNS Cont.(ps)	Fanout	Capacitance	Reference Model
C1	3	-900

Solutions

This algorithm can be used with implementation tool as well as sign-off tools. However, the accuracy of output is enhanced with sign-off tools. Those output reports may lead to following solutions,

- Setup:**
1. Increase the drive strength of the cell
 2. Select Low-VT reference for better timings
 3. Restructure the logic causing a timing Hot-Spot
 4. Resolve any placement or routing related issue near by the cell location
 5. Modify the timing constraints for the region

- Hold:**
1. Hold buffer can be added on reported nodes instead of each failing endpoint (This will save area and power)

Bottom Line

Time and efforts required to achieve timing closure can be reduced by using this algorithm. Quick identification of probable cause of multiple timing violation provide more time to decide solution that can resolve multiple violating endpoints. After first-cut Place and Route, analysis can be performed to identify timing hot-spots. Resolving issues near that region help in improving timing performance of whole design very quickly.

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