

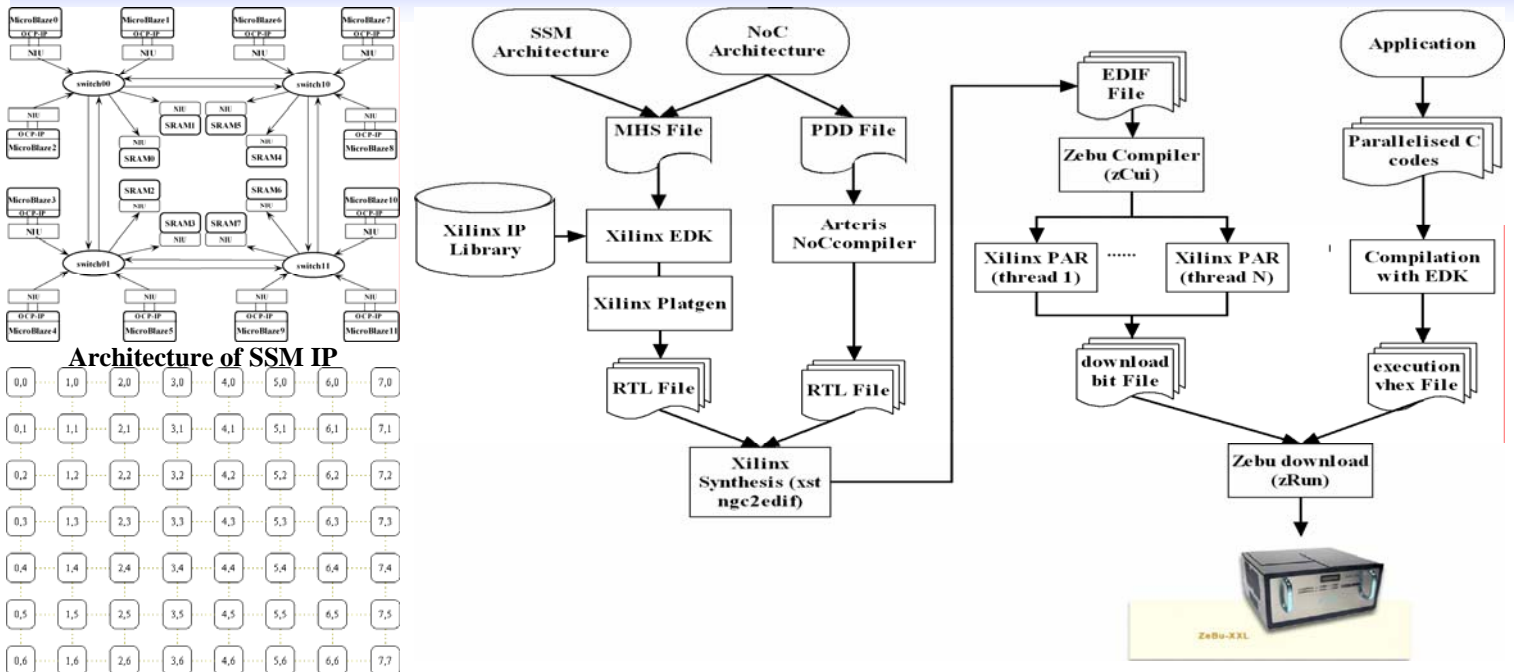
Context

- Future generation multiprocessor system on chip (MPSOC) will be based on hundreds of processors connected through network on chips.
- Mid-size and large scale Multiprocessor Design productivity is a major problem for system level design
- Lack of traffic behavior and patterns performance data on large scale multiprocessor
- Large scale emulation platform is the only tool for billion cycle evaluation in 'reasonable' performance evaluation time

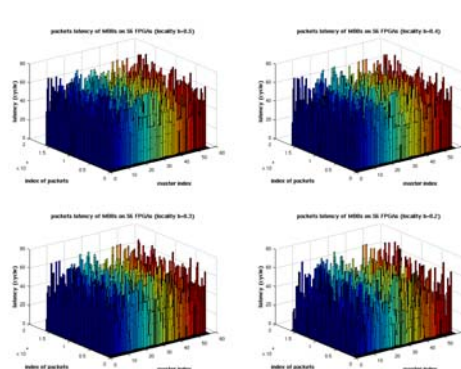
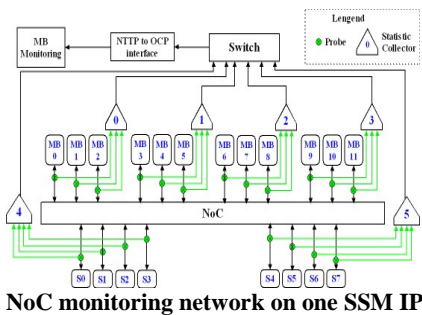
Objective

- Automatic Generation, Execution and Performance Monitoring of a Family of Multiprocessors on Large Scale Emulator
- Large scale NoC monitoring based on actual execution
- Analysis based on OCP-IP NoC micro-benchmarks
- Understanding of various patterns (hot spot, hot spot position, fork-join, etc) and feedback on parallel programmers
- NoC monitoring driven automatic parallel software DSE on large scale MPSOC

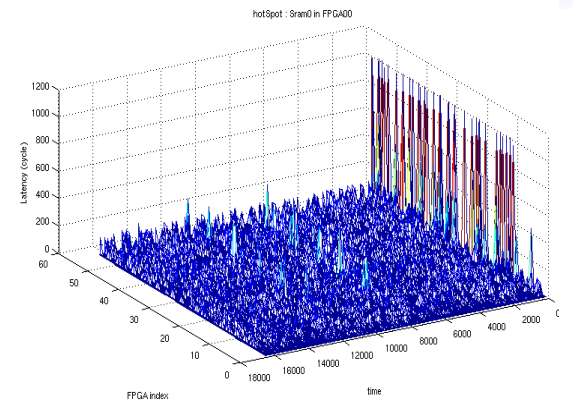
Automatic Multiprocessor Design Flow on Multi-FPGA platform



OCP-IP NoC Micro-benchmarks Performance Evaluation



Latency result of Locality benchmark



Latency result of Hot spot benchmark

References

1. A.A.Jerraya and W.Wolf, "Multiprocessor Systems-on-Chips", Morgan Kaufman Pub., 2004
2. K. Asonvic, RAMP: Research Accelerator for Multiprocessors, 2nd Workshop on Architectural Research Prototyping, WARP-2007
3. X.Li, O.Hammami, "Fast Design Productivity for Embedded Multiprocessor Through Multi-FPGA Emulation The case of a 48-way Multiprocessor with NOC", IP 08 Grenoble France Dec. 2008
4. X. Li, O.Hammami, "Multi-FPGA Emulation of a 48-core Multiprocessor with NOC", IDT 08 Monastir Tunisia Dec. 2008
5. Eve <http://www.eve.com>
6. OCP-IP Network-on-Chip Benchmarking Specification Part 1: Application modelling and hardware description v.1.0 May 23rd, 2008. <http://www.ocpip.org>
7. OCP-IP Network-on-Chip Benchmarking Specification Part 2: Micro-benchmark Specification v.1.0 May 23rd, 2008. <http://www.ocpip.org>