



Call for Papers

DSNOC'10



DAC Colocated Workshop on

Diagnostic Services in Network-on-Chips – 4th Edition

Test, Debug, and On-Line Monitoring

Anaheim, USA, June 13, 2010

DAC is the premier conference devoted to Electronic Design Automation (EDA) and the application of EDA tools in designing advanced electronic systems. The conference scope embraces tools, algorithms, and design techniques for all aspects of electronic circuit and system design. DAC includes plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, and workshops, as well as an user track and special sessions on innovative ideas and topics. Apart from the core Electronic Design Automation topics, DAC community is specially interested in the areas of design automation for many-core architectures, system prototyping technology and embedded software design and debug. Colocated Workshops are focusing on emerging research and application topics. At DAC 2010, one of the Colocated Workshops is devoted to **Diagnostic Services in Network-on-Chips**. This one-day event consists of a plenary keynote, special sessions, regular and poster presentations, and a panel session. It is the fourth edition of a sequence of successful events hosted by DATE in 2007 and 2009, and DAC in 2008.

WORKSHOP DESCRIPTION

Network-on-Chips (NoCs) are settling as a new on-chip communication paradigm. Diagnostic services, such as test, debug, and on-line monitoring, are becoming an important factor in designing next-generation NoC-based systems. The NoC infrastructure itself requires diagnostic services, and can also be used to support those for the entire system. Although significant research has been done in NoC design, there are many open and pressing issues regarding diagnostic services. The focus of this workshop is to explore them and their implications on system design.

TOPIC AREAS

You are invited to participate and submit your contributions to the workshop on **Diagnostic Services in Network-on-Chips**. The area of interest is described by, but not limited to, the following topics:

- *Manufacturing test of NoC and NoC-based systems*
- *NoC fault and error modelling*
- *On-line monitoring of NoC reliability and performance*
- *Verification of NoC-based systems*
- *NoC test benchmarking*
- *Fault-tolerance approaches to NoC design*
- *Reconfiguration for fault tolerance and diagnostics*
- *Silicon debug and diagnosis of NoC infrastructure*
- *Tools and methods to NoC diagnostic services*
- *Debug for OS and application software*

SUBMISSION INSTRUCTIONS

Submissions are invited in the form of extended abstracts not exceeding 2 pages in IEEE conference style and must be submitted for selection as PDF file to <submissions@dsnoc.org>. All submissions will be evaluated with regard to their suitability for the workshop, originality, and technical soundness. Submissions can be accepted for regular or poster presentation. No formal proceedings will be published, but an electronic Informal Digest of Contributions will be made available to all workshop participants with all material that authors are willing to provide: papers, abstract, slides, posters, etc.. Authors of selected papers will be invited to submit an extended version of their work to a special issue of the Microprocessors and Microsystems Journal (MICPRO), printed by Elsevier.

Paper Submission deadline	March 26, 2010
Notification of Acceptance	April 23, 2010
Camera-Ready Material due date	May 21, 2010

MORE INFORMATION

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