

## ***Synergies in IC Design: PDKs and DFM Standards Working Together***

***Monday June 6, 8:30AM – 12:30PM, Room 29AB***

The complexity of rules and processes needed to ensure the manufacturability of ICs is increasing rapidly with every new technology node. Many of the issues involving Process Design Kits (PDK's) and Design for Manufacturability (DFM) are interrelated and can be simplified, if not eliminated, by standardized industry practices. This workshop will highlight those interrelated standards and showcase the ongoing work being done by industry leaders in solving these problems.

PDKs are the fundamental building blocks for all electronic design. Standardized representation of PDK content and interfaces will offer operating efficiencies to foundries, EDA companies, IP providers and design companies who use the PDK's, create their own kits or need to modify those that they receive from their foundries. Resultant PDK's are expected to be more robust and portable than ever before.

In the DFM arena, standardization has proceeded along 2 parallel fronts. In physical DFM, a standard high-level DFM verification and optimization language called OpenDFM has been defined to support the needs of manufacturability and PDK generation. OpenDFM rules bridge the gap between a layout style that allows only a few, very restricted layout patterns and a style that allows purely arbitrary layouts. Second, there is ongoing effort to standardize a common format for representing parasitic information and to better handle manufacturing variability. This has implications in how this data is represented in PDK's and how they affect the modeling of design parameters for power, timing and SI analysis.

### ***Synergies in Industry Practices: How PDKs and DFM Standards Can Work Together***

***8:30 AM - 09:00AM Registration & Breakfast***

***9:00 AM - 09:10AM Welcome and Introduction, Sumit DasGupta, Si2***

#### ***09:10AM - 10:40AM OpenPDK Session***

***09:10AM - 09:40PM: OPDK Coalition Overview, Robert Hum, MentorGraphics***

***09:40AM - 10:10AM: Open Process Spec Progress: Gilles Namur, STMicroelectronics***

***10:10AM - 10:40AM: Symbols, CDF, and Callback Progress: Rich Morse, Springsoft***

***10:40AM - 11:00AM: Break***

#### ***11:00AM - 12:30PM OpenDFM Session***

***11:00AM - 11:30AM: 2011 OpenDFM Overview, A Customer Perspective, Fred Valente, TI***

***11:30AM - 12:00PM: Targeting and Litho Bias, Bob Sayah, IBM***

***12:00PM - 12:30PM: Parasitic Extraction Standards and Design for Variability, Concetta Riccobene, LSI***