DESIGN AUTOMATION CONFERENCE

June 13-18, 2010
Anaheim Convention Center

Sponsored by:

SIGDA

CEDA
IEEE Council on Electronic Design Automation

EDA CONSORTIUM

In technical cooperation with:

SSCS

www.dac.com

PROGRAM GUIDE

GENERAL CHAIR'S WELCOME

LET'S MEET AT DAC!

Dear Colleague:

The 47th edition of the Design Automation Conference in Anaheim is just around the corner, and I look forward to welcoming you there. As the central "meeting place" for electronic design and design automation where the industry puts on its grand annual show, there are many facets to DAC. It's the place new contacts are made, where deals are sealed, where theory meets practice, where colleagues across the industry network, where the seeds of great new ideas are sowed – and much more. DAC is our annual signpost that points the way to the future.

As organizers of the event, we work with DAC's sponsors and hundreds of volunteers to make it worth your time to attend. This year, in addition to reinforcing traditional strengths, we have added a number of exciting new elements. Here's a sample of what you can see at DAC:

- The **keynote** lineup features three distinguished and accomplished industry luminaries: Doug Grose, CEO of GLOBALFOUNDRIES will address the central role of the foundry in electronic design on Tuesday. Bernie Meyerson, Vice President for Innovation at IBM Corporation, will discuss his vision for next-generation IT infrastructure for EDA and the move towards cloud computing, and Iqbal Arshad, Corporate Vice President of Innovation Products at Motorola, will overview his experiences in driving the Motorola Droid from concept to product.
- A vibrant **exhibition** showcases nearly 200 companies, including all of the largest EDA vendors and a significant foundry presence. The Exhibitor Forum theater features focused technical presentations from exhibitors, while IC Design Central's exhibit area and a presentation stage that brings together the entire ecosystem for SOC enablement, including IP providers, design services provides, and foundries.
- A special **Embedded/SOC Enablement Day** on Thursday is designed to further advance DAC's partner eco-system, attracts a mix of chip creators, ecosystem suppliers, and research-focused participants.
- A robust and exciting **technical program** includes an exciting array of panels and special sessions that complement a carefully selected subset of the contributed research papers.
- The **User Track** program, specifically designed by and for EDA tool users, features presentations and poster sessions that highlight outstanding solutions to critical design and methodology challenges, and case studies of innovative tool use. In its second year, it is 50% larger than last year's acclaimed program.
- An excellent slate of **tutorials** covers topics such as low-power design, ESL, and software development for the EDA professional.
- **Management Day** includes invited presentations and networking opportunities for decision-makers in the industry, and highlights issues at the intersection of business and technology.
- An impressive constellation of fourteen **colocated events** and six **DAC workshops** complements the DAC program: this includes established conferences and symposia such as AHS, DFM&Y, DSNOC, HOST, HLDVT, NANOARCH, SASP, and SLIP, as well as meetings on emerging topics such as bio-design automation, mobile/cloud computing, and smart grids.

As you can see, there's tons of good stuff in store – come join us in Anaheim!

Sachin S. Sapatnekar
General Chair, 47th DAC

TECHNICAL PROGRAM HIGHLIGHTS

The technical program for DAC 2010 exceptional-quality technical papers, panels, special sessions, WACI (Wild and Crazy Ideas), full day tutorials and User Track. The program is tailored for researchers and developers in the electronic design and design automation industry, design engineers, and management. It highlights the advancements and emerging trends in the design of electronic circuits and systems.

The core of the technical program consists of 148 peer-reviewed papers selected from 607 submissions (a 24% acceptance ratio). Organized in 35 technical sessions, these papers cover a broad set of topics ranging from system-level design, low-power design, physical design and manufacturing, embedded systems, logic and high level synthesis, simulation, verification, test and emerging technologies.

Popular submission themes included:

1. Power Analysis and Low-Power Design (83 submissions, 5 sessions)
2. Physical Design and Manufacturability (72 submissions, 4 sessions)
3. System-Level Design and Analysis (69 submissions, 4 sessions)

Some of the novel ideas presented in these papers includes cutting-edge research in property checking, global routing, variation characterization, silicon mismatch, cache design for routers, rewiring, logic optimization with don't cares, Boolean matching, and low energy processor design. The papers reflect the increasing importance of system-level design, low-power design and analysis, and physical design and manufacturability.

KEYNOTES

TUESDAY
JUNE 15

FROM CONTRACT TO COLLABORATION: DELIVERING A NEW APPROACH TO FOUNDRY

Douglas Grose, Chief Executive Officer, GLOBALFOUNDRIES, Sunnyvale, CA

The list of challenges facing the semiconductor industry is daunting. Chip design continues to increase in complexity, driven by product requirements that demand exponentially more performance, functionality and power efficiency, integrated into a smaller area. In parallel, manufacturing technology is facing increased challenges in materials, cost and shorter product lifecycles. This confluence of factors puts the industry at a crossroads and the foundry industry at center stage.

Chip design companies need to redefine relationships with their manufacturing partners, and foundries must create a new model that brings manufacturing and design into an integrated and collaborative process. This presentation will explore the challenges of bringing the next generation of chip innovation to market through leveraging an integrated global ecosystem of talent and technology. The world's top design companies want more than a contract manufacturer; they want a level of collaboration and flexibility supported by a robust partner ecosystem of leading providers in the EDA, IP and design services sectors.

WEDNESDAY
JUNE 16

ECHOES OF DAC'S PAST: FROM PREDICTION TO REALIZATION, AND WATTS NEXT?

Bernard S. Meyerson, IBM Fellow, Vice President-Innovation, IBM Corp., Yorktown Hts., NY

Over the last five years the semiconductor industry has acknowledged, but struggled to deal with, the end of classical device scaling in silicon technology. This has had ramifications across all aspects of the technology spectrum, as a steady stream of innovations, ever more fundamental, have been required to drive accustomed generational improvements in Information Technology (IT). Adding to this challenge on the demand side there has been an accelerating and seemingly insatiable need for IT resources, driven by the emergence of the 'Internet of Things'. With such heavy and growing IT demands, key metrics such as system power, cost/performance, and application specific benchmarks have become a core focus of emerging solutions. It is these same metrics and constraints that also require advances in the efficiency and optimization of IT. In this talk, I will review how our industry is dealing with each of these challenges, and explore emerging compute paradigms, such as Cloud Computing, that are impacting EDA directly.

THURSDAY
JUNE 17

DESIGNING THE MOTOROLA DROID

Iqbal Arshad, Corporate VP, Innovation Products, Motorola Mobile Devices, Inc., Schaumburg, IL

As mobile internet usage skyrockets and more sophisticated mobile applications are being developed, the device formerly known as the cell phone is at a major technological inflection point. To meet this challenge, we must design devices and services that enable a transformation in the way we work, socially interact, use the web and utilize computing power. A key ingredient to making this happen is the synthesis of new hardware that is tightly coupled with a new software experience or business opportunity. Similarly, when launching new high-technology products, the success of the product largely depends on how well the target consumer is educated about the availability and capability of the new device. This talk will discuss how designing the Droid helped Motorola to address this shift in the market place.

USER TRACK

Sponsored by:

The DAC User Track brings together IC designers from across the globe. The User Track program offers a unique opportunity to pick up the latest tips and tricks from the industry expert IC designers, and features over 110 presentations on a wide variety of topics. Designers from Intel, IBM, Samsung, TI, Toshiba, Qualcomm, AMD, Freescale and other leading IC companies will present their experiences on building effective design flows, design methods, and tool usage. Come to DAC to attend the User Track - there is no other way to improve your 'design IQ' in just a short amount of time!

The list of topics is longer and more diverse than ever, and there is something in the User Track for every designer. Low-power design is one of the core topics addressed at the system-level, RTL, and during the place-and-route stages of design. The User Track features talks on efficient design for low-power and on power delivery on the chip and through the package. In other talks, designers will address dealing with the significant variability at 32nm and below. You will find interesting presentations on variation-robust design methods, with ways to quickly converge on high-yield designs. Timing closure is another theme that is addressed by speakers from a several perspectives, both front-end and back-end. Designers will present innovative ways for partitioning, budgeting and retiming. Also featured are presentations on several timing-driven ECO physical optimization methods, and system-level case studies that use formal verification and much more. Please check out the program in the new dac.com website for the full details on the presentations.

The Design Automation Conference and the User Track bring together thousands of like-minded professionals, making this event an opportunity you cannot miss. The User Track runs for three packed days as a parallel track within the DAC technical program. Learn from expert designers in person, and find out the truth about design tools. Stroll through the DAC trade show, attend keynotes and cutting-edge technical sessions, or just talk to colleagues from other companies. Whether it's for the full three days or just a single day, DAC has it all. And since DAC 2010 is held right next to Disneyland, this is a great opportunity to bring your family along.

USER TRACK SESSIONS

- Timing is Everything
- Front-End Design Experiences
- Taming Back-End Verification and DFM
- Case Studies in Formal Verification
- Cornered: Dealing with Variability
- Front-End Testing and Verification
- Power Delivery from Package to Chip
- Advances in System-Level Design and Synthesis
- User Track Poster Sessions

MANAGEMENT DAY

Tuesday, June 15

Sponsored by:

Management Day 2010 is focused on issues at the intersection of business and technology, and is specifically directed to managers and decision-makers. Three sessions make up this year's event. Two sessions will feature managers representing IDMs, fablight ASIC providers, and fabless companies, as well as senior managers designing today's most complex nanometer chips, and will discuss the latest solutions and their economic impact. The third session will be a panel that involves the presenters and the audience in a brainstorming discussion.

EMBEDDED/SOC ENABLEMENT DAY

Thursday, June 17

The Embedded/SoC Enablement Day is dedicated to bringing industry stakeholders together in one room to shed light on where SoC design is headed. The event comprises presentations from leading SoC enabling sectors including embedded processors, embedded systems, EDA, FPGA, IP, foundry, and design services. Presenters will focus on the optimization of embedded and application-domain-specific operating systems, system architectures for future SoCs, application-specific architectures based on embedded processors, and technical/business decision making processes by program developers. This program consists of three sessions, and provides an opportunity to foster discussions that address all aspects of the SoC development ecosystem.

TUTORIALS

The DAC program includes seven tutorials on timely subjects, including four design topics: 3-D integrated circuits, analog mixed-signal design, system-level design, and low-power design. This year also features tutorials on two special topics. The first is an overview of software engineering that includes introductions to agile, lean, scrum, and other software best practices—topics that will offer immediate and practical value to students, EDA developers, and SOC firmware engineers. The second is a tutorial on the importance of effective marketing and should appeal to a broad range of DAC attendees that wish to better understand this aspect of business success. As in the past, the goal of the DAC tutorials is to provide practical, usable, and up-to-date knowledge that attendees can immediately apply in their jobs or studies.

MONDAY TUTORIALS

- ESL Design and Virtual Prototyping of MPSOCs
- Low-Power from A to Z
- Marketing of Technology - The Last Critical Step

FRIDAY TUTORIALS

- 3-D: New Dimensions in IC Design
- Advancing the State-of-the-Art in Analog Circuit Optimizers
- Best Practices for Writing Better Software
- SystemC for Holistic System Design with Digital Hardware, Analog Hardware, and Software

Detailed conference and exhibition information is now available online: www.dac.com.

Register today!

QUESTIONS? Call +1-303-530-4333

PANELS

This year's DAC panels cover nearly every aspect of the design flow. The panel sessions start off with a look to the future by a wide range of leaders from the semiconductor industry. The other seven panels have something for everyone. Panels will explore the future of TSV/3D technology, the current state of high-level synthesis, different approaches to addressing process variability, the future of low-power design methodologies and how to bridge pre-silicon verification/post-silicon validation. One panel will also take a look at what is needed for an always-connected car. Finally, if you've wondered what cloud computing is all about, a panel will explore how cloud computing fits in with the EDA industry.

TUESDAY, JUNE 15

- EDA Challenges and Options: Investing For the Future
- Bridging Pre-Silicon Verification and Post-Silicon Validation
- Who Solves the Variability Problem?

WEDNESDAY, JUNE 16

- 3-D Stacked Die: Now or the Future?
- Does IC Design Have a Future in the Clouds?
- What's Cool for the Future of Ultra Low-Power Designs?

THURSDAY, JUNE 17

- Designing the Always-Connected Car of the Future
- Joint User Track Panel - (Session 8UB) - What Will Make Your Next Design Experience a Much Better One?
- What Input Language is the Best Choice for High-Level Synthesis (HLS)?

SPECIAL SESSIONS

Special sessions will deal with a wide variety of themes such as progress in networks-on-chip research, virtualization for mobile embedded devices, challenges in analog modeling, introduction to cyber-physical systems, design for reliability, designing resilient systems from unreliable components, a holistic view on energy management – cell phones to power grids and post-silicon validation. Leading research and industry experts will present their views on these topics.

TUESDAY, JUNE 15

- Post-Silicon Validation or Avoiding the $50 Million Paperweight
- Virtualization in the Embedded Systems: Where Do We Go?
- Joint DAC/IWBDA Special Session - Engineering Biology: Fundamentals and Applications

WEDNESDAY, JUNE 16

- A Decade of NOC Research - Where Do We Stand?
- The Analog Model Crisis - How Can We Solve It?
- Design Closure for Reliability

THURSDAY, JUNE 17

- WACI: Wild and Crazy Ideas
- Cyber-Physical Systems Demystified
- Computing Without Guarantees
- Smart Power: From your Cell Phone to your Home

WORKSHOPS

SUNDAY, JUNE 13

- DAC Workshop on Synergies between Design Automation & Smart Grid
- Multiprocessor System-On-Chip (MPSOC): Programmability, Run-Time Support and Hardware Platforms for High Performance Applications at DAC
- DAC Workshop on Diagnostic Services in Network-On-Chips (DSNOC) - 4th Edition

MONDAY, JUNE 14

- IWBDA: International Workshop on Bio-Design Automation at DAC
- DAC Workshop on "Mobile and Cloud Computing"
- DAC Workshop: More Than Core Competence...What it Takes for Your Career to Survive, and Thrive! Hosted by Women in Electronic Design (WWED)

COLOCATED EVENTS

FRIDAY, JUNE 11

- IEEE International High-Level Design Validation and Test Workshop (HLDVT 2010)

SUNDAY, JUNE 13

- International Symposium on Hardware-Oriented Security and Trust (HOST)
- 8th IEEE Symposium on Application Specific Processors (SASP 2010)
- Design for Manufacturability Coalition Workshop - "A New Era for DFM"
- IEEE/ACM 12th International Workshop on System-Level Interconnect Prediction (SLIP)
- North American SystemC Users Group (NASCUG 13 Meeting)
- System and SOC Debug Integration and Applications

MONDAY, JUNE 14

- 4th IEEE International Workshop on Design for Manufacturability & Yield (DFM&Y)
- Choosing Advanced Verification Methods: So Many Possibilities, So Little Time
- Advances in Process Design Kits Worshop

TUESDAY, JUNE 15

- ACM Research Competition
- NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2010)

THURSDAY, JUNE 17

- IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH'10)

FRIDAY, JUNE 18

- 19th International Workshop on Logic & Synthesis (IWLS)

EXHIBITOR LIST (AS OF APRIL 12, 2010)

Accelicon Technologies, Inc.
ACCIT - New Systems Research
ACE Associated Compiler Experts bv
Agilent Technologies
Agnisys, Inc.
Aldec, Inc.
Altair Engineering
Altos Design Automation
Amiq Consulting S.R.L.
AnaGlobe Technology, Inc.
Analog Bits Inc.
Apache Design Solutions, Inc.
Applied Simulation Technology
Artwork Conversion Software, Inc.
ASIC Analytic, LLC
ATEEDA
Atoptech
Atrenta Inc.
austriamicrosystems
AutoESL Design Technologies, Inc.
Avant Technology Inc.
Avery Design Systems, Inc.
Axiom Design Automation
BEEcube, Inc.
Berkeley Design Automation, Inc.
BigC
Blue Pearl Software
Bluespec, Inc.
Breker Verification Systems
Cadence Design Systems, Inc.
Calypto Design Systems
Cambridge Analog Technologies
CAST, Inc.
ChipEstimate.com
Ciranova, Inc.
CISC Semiconductor Design+Consulting GmbH
ClioSoft, Inc.
CMP
CoFluent Design
Concept Engineering GmbH
Coupling Wave Solutions
CST of America, Inc.
DAC Pavilion
Dassault Systemes Americas Corp.
DATE 2011
Denali Software, Inc.
Design and Reuse
Dini Group
DOCEA Power
Dorado Design Automation, Inc.
Duolog Technologies Ltd.
E-System Design
EDA Cafe-IB Systems
EDXACT SA
Entasys Inc.
Enterpoint Ltd.
EVE-USA, Inc.
Exhibitor Forum
ExpertIO, Inc.
Extension Media LLC
Extreme DA
FishTail Design Automation, Inc.
Forte Design Systems
Gary Stringham & Associates, LLC
GateRocket, Inc.
GiDEL
Global Foundries
Gradient Design Automation
Helic, Inc.
Hewlett-Packard Co.
HiPEAC
IBM Corp.
IC Manage, Inc.
ICDC Partner Pavilion & Stage
IMEC - Europractice
Imera Systems, Inc.
Infotech Enterprises
iNoCs
Interra Systems, Inc.
Jasper Design Automation, Inc.
Jspeed Design Automation, Inc.
JTAG Technologies
Laflin Limited
Legend Design Technology, Inc.
Library Technologies, Inc.
Lynguent, Inc.
Magillem Design Services
Magma Design Automation, Inc.
Magwel NV
MathWorks, Inc. (The)
Menta
Mentor Graphics Corp.
Mephisto Design Automation
Methodics LLC
Micro Magic, Inc.
Micrologic Design Automation, Inc.
Mirabilis Design Inc.
Mixel, Inc.
MOSIS
MunEDA GmbH
Nangate
NextOp Software, Inc.
Nusym Technology, Inc.
Oasys Design Systems, Inc.
OneSpin Solutions GmbH
OptEM Engineering Inc.
OVM World
Physware, Inc.
PLDA
POLYTEDA Software Corp.
Progate Group Corp.
Prolific, Inc.
Pulsic Inc.
R3 Logic Inc.
Rapid Bridge, LLC
Real Intent, Inc.
Reed Business Information
RTC Group - EDA Tech Forum
Runtime Design Automation
Sagantec
Sapient Systems
Satin IP Technologies
Seloco, Inc.
Semifore, Inc.
Si2
Sigrity, Inc.
Silicon Design Solutions
Silicon Frontline Technology
SKILLCAD Inc.
Solido Design Automation
Sonnet Software, Inc.
Springer
SpringSoft, Inc.
StarNet Communications
Synapse Design
Synchronicity - see Dassault Systèmes
Synfora, Inc.
Synopsys, Inc.
Synopsys, Inc. - Standards Booth
Synopsys-ARM-Common Platform Innovation
SynTest Technologies, Inc.
Tanner EDA
Target Compiler Technologies NV
Teklatech
Tela Innovations
Tiempo
TOOL Corp.
True Circuits, Inc.
TSMC
TSMC Open Innovation Forum, Apache
TSMC Open Innovation Forum, Cadence
TSMC Open Innovation Forum, eSilicon
TSMC Open Innovation Forum, Helic, Inc.
TSMC Open Innovation Forum, Integrand
TSMC Open Innovation Forum, Lorentz
TSMC Open Innovation Forum, Magma
TSMC Open Innovation Forum, Mentor
TSMC Open Innovation Forum, MoSys
TSMC Open Innovation Forum, Solido
TSMC Open Innovation Forum, SpringSoft
TSMC Open Innovation Forum, Synopsys
TSMC Open Innovation Forum, Tela Innovations
TSMC Open Innovation Forum, Virage Logic
TSSI - Test Systems Strategies, Inc.
Tuscany Design Automation, Inc.
UMC Research Centre
Uniquify, Inc.
Univa UD
Vennsa Technologies, Inc.
Verific Design Automation
Veritools, Inc.
WinterLogic Inc.
X-FAB Semiconductor Foundries
XJTAG
XYALIS
Z Circuit Automation
Zocalo Tech, Inc.

Orange text denotes a new exhibitor

Platinum Exhibitors

cadence

SYNOPSYS®

Gold Exhibitors

Apache Design Solutions

denali

GLOBALFOUNDRIES

Mentor Graphics

tsmc

Silver Exhibitors

ATRENTA

SpringSoft accelerating engineers

EXHIBITION

The 47th DAC exhibition is located in Halls B and C of the Anaheim Convention Center.

Visit the DAC exhibition for an in-depth view of new products and services from nearly 200 vendors spanning all aspects of the electronic design process, including EDA tools, IP cores, embedded system and system-level tools, as well as silicon foundry and design services.

EXHIBITOR FORUM

DAC is continuing the popular Exhibitor Forum again this year. The Exhibitor Forum provides a theater on the exhibit floor where exhibitors present focused, practical technical content to attendees. The presentations are selected by an all-user Exhibitor Forum Committee chaired by Magdy Abadir of Freescale Semiconductor, Inc. Each session is devoted entirely to a specific domain (e.g., verification or system-level design) and consists of presentations from three companies.

The Exhibitor Forum is in Hall B in Booth 1684. Topics include: System-Level Design/Embedded Software, Physical Design and Sign-Off, Verification, Power Management/Signal Integrity, Analog/Mixed-Signal and RF, Design for Manufacturability, Intellectual Property Cores, Design for Test and Manufacturing Test, Package Design, and Silicon Validation and Debug.

DAC PAVILION

Sponsored by: GLOBALFOUNDRIES

The popular DAC Pavilion is located in Hall C in Booth 694. The DAC Pavilion will feature 17 presentations on business and technical issues.

MONDAY, JUNE 14

- Gary Smith on EDA: Trends and What's Hot at DAC
- The Multiplier Effect: Developing Multi-Core, Multi-OS Applications
- Career Outlook: Job Market 2010
- Outsourcing...!@#$*&!!?
- EDA Heritage - Meet Verilog Inventor Dr. Moorby and Formal Verification Pioneer Prof. Bryant
- A Conversation with the 2010 Marie Pistilli Award Winner

TUESDAY, JUNE 15

- Hogan's Heroes: What Design and Lithography Nightmares will 22nm Bring?
- Everyone Loves a Teardown (ARM)
- Is the FPGA Tool Opportunity an Oasis or a Mirage?
- 28nm and Below: SOC Design Ecosystem at a Crossroad
- Hot and SPICEy: Users Review Different Flavors of SPICE and Fast SPICE

WEDNESDAY, JUNE 16

- Lucio's Litmus Test: Is Your Start-Up Ready for the 21st Century?
- IP Commercialization: Beyond the Code
- Everyone Loves a Teardown (Virage Logic)
- High-School Panel: You Don't Know Jack!
- Analog Interoperability: What's the ROI?
- SOC Verification: Are We There Yet?

THE IC DESIGN CENTRAL PARTNER PAVILION—PUTTING MORE DESIGN INTO DAC

The IC Design Central Partner Pavilion, located in Hall B, stage #1710, brings together vendors supplying products and services that address many of the critical design functions necessary to produce working silicon on time and on budget. Companies from all areas of the design and product development process—EDA, Foundry, IP, Design Services, Assembly/Package, Test, and System Interconnect—must cooperate to offer integrated front-to-back solutions that ensure first-time-successful silicon and predictable time-to-market. Visit the ICDC Partner Pavilion and find design flows and solutions needed to create today's challenging designs.

The ICDC Partner Pavilion is a combination of exhibit booths and 30-minute presentations by each participating vendor. The combination of product displays in the exhibits and technical product presentations in the ICDC Theater offers attendees an in-depth look into flows and methodologies from vendors featuring a variety of products and services for the entire design ecosystem.

CURRENT PARTICIPATING ICDC EXHIBITORS INCLUDE:

Altair Engineering
Amiq Consulting S.R.L.
ASIC Analytic, LLC
Avant Technology Inc.
BEEcube, Inc.
Cambridge Analog Technologies
CoFluent Design
CISC Semiconductor Design & Consulting
Enterpoint Ltd.
ExpertIO, Inc.
Gary Stringham & Associates, LLC
IBM Corp.
iNoCs
Progate Group Corp.
R3 Logic Inc.
TSSI - Test Systems Strategies, Inc.
X-FAB Semiconductor Foundries
Zocalo Tech, Inc.

EXHIBIT-ONLY PASS

Register for an exhibit-only pass and receive admission to all days of the exhibition, all Keynotes, all DAC Pavilion and Exhibitor Forum sessions, the IC Design Central Partner Pavilion, plus the Tuesday night DAC party, and a T-shirt —all for $50 when you register by May 17.

EXHIBITION HOURS

MONDAY, JUNE 14 - WEDNESDAY, JUNE 16

9:00am - 6:00pm

Register Online by May 17 and Save!

REGISTRATION OPTIONS:

Internet registration is open through June 18. Mail/fax registrations are accepted through June 8.

FULL CONFERENCE REGISTRATION includes: access to all three days of the Technical Sessions, User Track Sessions, Embedded/SOC Enablement Day, access to the Exhibition, Monday through Wednesday, the 47 Years of DAC DVD Proceedings and the Tuesday Night Party.

STUDENTS FULL CONFERENCE REGISTRATION IEEE MEMBER OR ACM MEMBER
A special student rate applies to individuals who are members of ACM or IEEE and are currently enrolled in school. Students must provide a valid ACM or IEEE student membership number and a valid student ID. ACM/IEEE Student registration includes: all three days of the Technical Conference, Embedded/SOC Enablement Day, access to the Exhibition, Monday through Wednesday, the 47 Years of DAC DVD Proceedings and the Tuesday Night Party.

ONE/TWO DAY REGISTRATION INCLUDES: include the day(s) you select for the Technical Conference, access to the Exhibition, User Track (UT) Sessions, Monday through Wednesday, and the "47 Years of DAC" DVD Proceedings.

EXHIBIT-ONLY REGISTRATION allows admittance to the Exhibition, Monday through Wednesday and includes the Tuesday Night Party.

USER TRACK SESSIONS registration includes entrance to the Exhibition, Monday through Wednesday and all Keynotes. User Track Sessions are included in the Full Conference registration and the One-/Two-day registration on the day(s) attending the technical conference.

MANAGEMENT DAY registration for this event includes entrance to the Exhibition, Monday through Wednesday, and all Keynotes.

TUTORIALS are offered on Monday, June 14 and Friday, June 18. There is one quarter-day tutorial, two half-day tutorials, and four full-day tutorials. The full-day tutorial registration fee includes: continental breakfast, lunch, refreshments and tutorial notes. The half-day tutorial registration fee includes: continental breakfast, refreshments and tutorial notes. The quarter-day tutorial registration fee includes: refreshments and tutorial notes.

EMBEDDED/SOC ENABLEMENT DAY is a day-long track of sessions dedicated to bringing industry stakeholders together in one room to shed light on where SOC design is headed. The day is comprised of presentations from leading SOC enabling sectors, including embedded processors, embedded systems, EDA, FPGA, IP, foundry, and design services.

WORKSHOPS/COLOCATED EVENT registration also includes entrance to the Exhibition, Monday through Wednesday.

Visit the DAC website for online registration, complete conference and exhibition details, travel and hotel reservations and information on visiting Anaheim at www.dac.com.

CANCELLATION/REFUND POLICY:
Written requests for cancellations must be received in the DAC office by Monday, May 17, 2010 and are subject to a $25.00 processing fee. Cancellations received after May 17, 2010 will NOT be honored and all registration fees will be forfeited. No faxed or mailed registrations will be accepted after June 8, 2010.

Telephone registrations are not accepted!

Faxed or mailed registrations without payment will be discarded.

User Track

User Track Sessions	$185	$240

Tutorials

Full-day	$300	$400	$200
Half-day	$180	$240	$120
Quarter-day	$100	$130	$80

Workshops at DAC

DAC Workshop on Diagnostic Services in Network-on-Chips (DSNOC) - 4th Edition	Sunday, June 13	$150	$195
Multiprocessor System on Chip (MPSOC): Programmability, Run-Time Support and Hardware Platforms for High Performance Applications at DAC			
DAC Workshop on Synergies between Design Automation & Smart Grid			
DAC Workshop: More Than Core Competence...What it Takes for Your Career to Survive, and Thrive! Hosted by Women in Electronic Design (WWED)	Monday, June 14	**FREE** up to 100 attendees	
DAC Workshop on "Mobile and Cloud Computing"		$150	$195
International Workshop on Bio-Design Automation at DAC (IWBDA)	Monday, June 14 & Tuesday, June 15	$230	$305

Conference Registration Rates

	Advance Rate Received by May 17			Late/On-site Rate Received After May 17		
Full Conference	$475	$595	$230	$570	$695	$295
One-Day Only (Tue., Wed., Thurs.)	$325			$325		
Two-Day Only (Tue, Wed., Thurs.)	$525			$525		
Exhibit-only access all days (Mon. - Wed.)	$50			$95		
Monday Exhibit-only (Monday)	**FREE**			**FREE**		
Management Day (Tuesday)	$95			$95		
Embedded/SOC Enablement Day	$95			$95		

ACM/IEEE Member
ACM/IEEE Student Member
Non-member
Student Non-member

Colocated Events at DAC

	Dates	Advance Registration				Late/Onsite Registration			
IEEE International High Level Design Validation and Test Workshop 2010 (HLDVT)	Fri. June 11 - Sat., June 12	$350	$450	$250	$250	$450	$575	$300	$300
IEEE/ACM 12th International Workshop on System Level Interconnect Prediction (SLIP)	Sun., June 13	$250	$320	$200	$200	$300	$370	$250	$250
Design for Manufacturability Coalition Workshop		**FREE**							
IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)	Sun., June 13 - Mon., June 14	$300	$375	$150	$190	$360	$450	$180	$225
8th IEEE Symposium on Application Specific Processors (SASP 2010)		$315	$410	$190	$190	$420	$530	$245	$245
4th IEEE International Workshop on Design for Manufacturability & Yield (DFM&Y)	Mon., June 14	$150	$200	$100	$150	$200	$250	$130	$200
Advances in Process Design Kits Workshop		**FREE**							
NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2010)	Tue., June 15 - Fri., June 18	$560	$560	$410	$410	$690	$690	$510	$510
IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH'10)	Thurs., June 17 & Fri., June 18	$285	$375	$225	$300	$350	$440	$240	$315