March 1, 2010

Failure Analysis-Driven Design for Manufacturability

Puneet Sharma, Chi-Min Yuan

PuneetSharma@freescale.com, **Chi-Min.Yuan@freescale.com**

Design for Manufacturability, Freescale, Austin TX

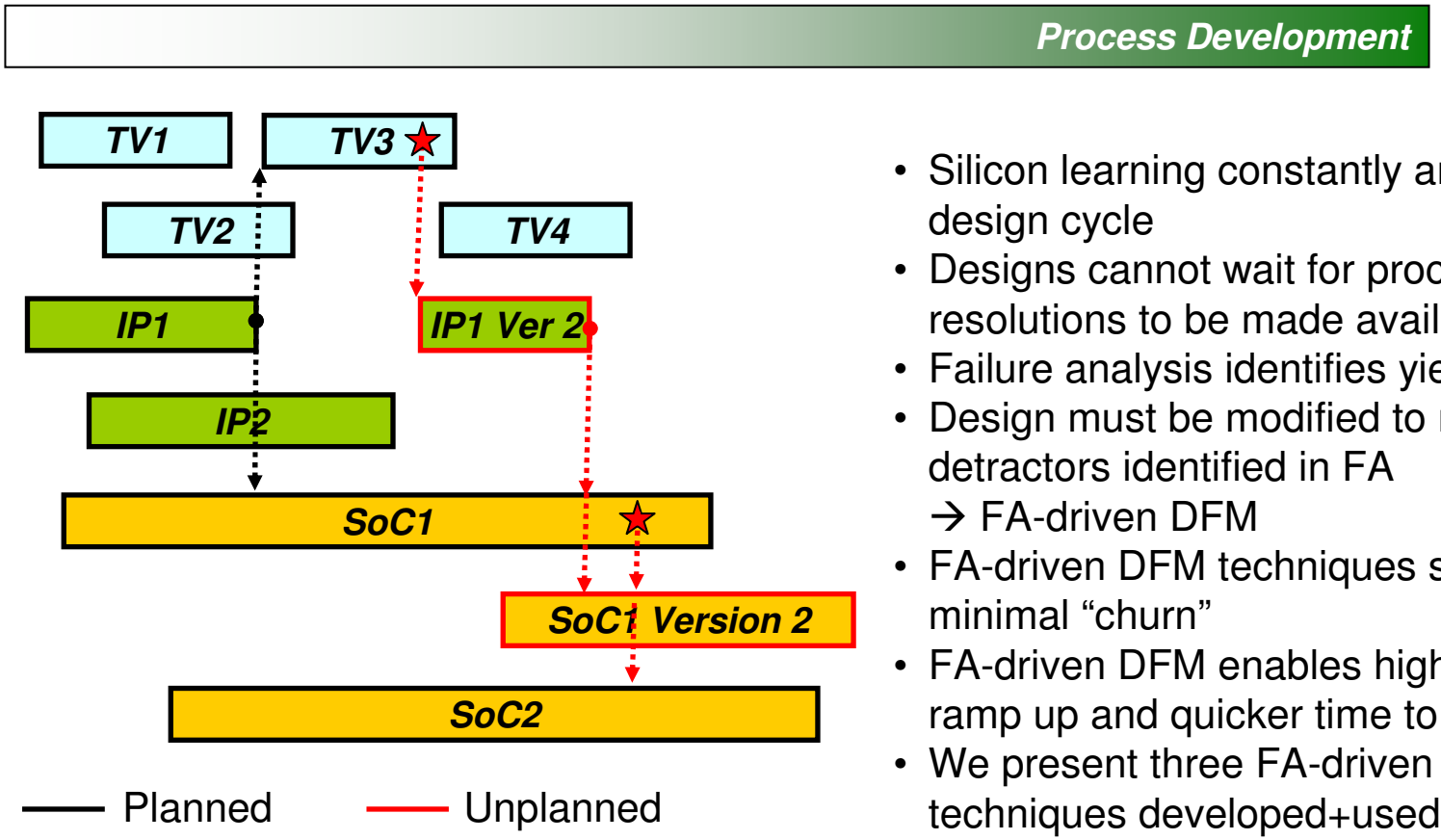
freescale™ semiconductor

Outline

- Motivation for FA-driven DFM
- Avoiding min. area metal shapes
- Mitigating via voids at line ends
- Late breaking litho hotspot fixing
- Summary

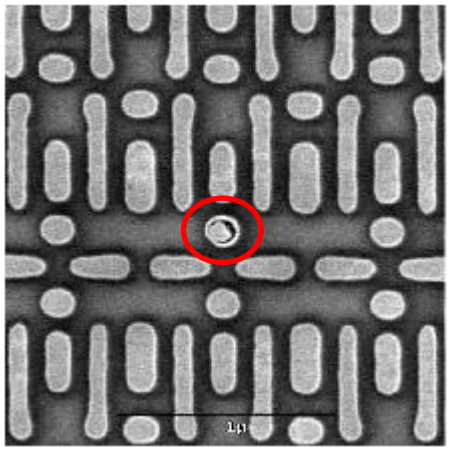
Failure Analysis-Driven DFM

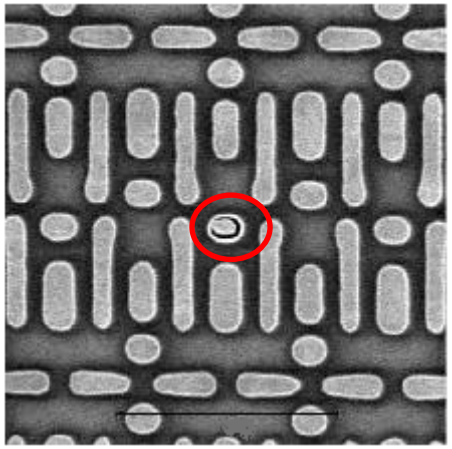
- Advanced technologies have long yield ramp up and design cycle time
- To shorten time to market, design begins much before process is mature for high volume production



- Silicon learning constantly arriving during design cycle
- Designs cannot wait for process resolutions to be made available
- Failure analysis identifies yield detractors
- Design must be modified to mitigate yield detractors identified in FA
  → FA-driven DFM
- FA-driven DFM techniques should cause minimal “churn”
- FA-driven DFM enables higher yield in ramp up and quicker time to market
- We present three FA-driven DFM techniques developed+used at Freescale

Minimum Area Metal





- Small metal shapes challenging for lithography and Cu plating tools
- Min area design rules prevents metal shapes below a threshold
  - But, small area shapes above threshold may not manufacture reliably → become yield detractors
- Failure analysis found a number of failures due to small metal shapes
  - Products with higher number of small area shapes had lower yield
- Improvements in plating equipment and chemical refresh rate nether cost effective nor adequate

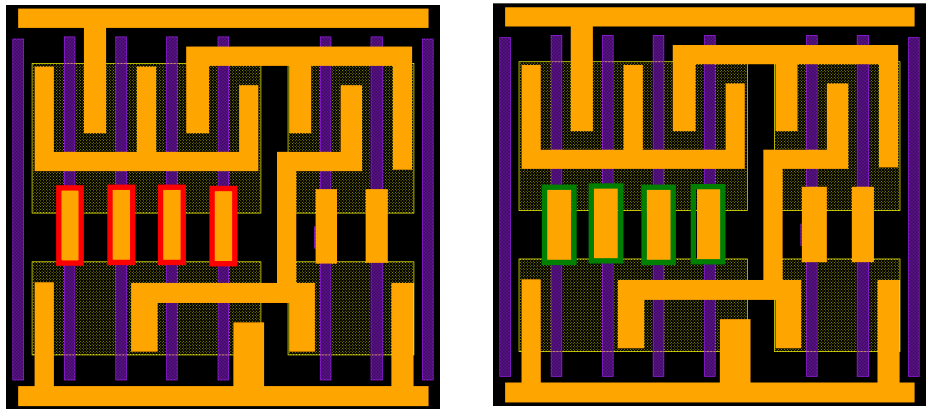
  → DFM solution desired that reduces number of small area shapes

IP-Level Optimization

- Primary contributors:
  - Memories
  - Standard cells
  - Routed interconnects

- Memories: no optimization done
  - Highly optimized → no space to increase area of small metal shapes
  - Layout modifications kickoff extensive Si characterization → impacts product tapeout schedule
  - Repair capability provides robustness

- Standard cells
  - Optimization focused on most frequently used cells
  - Physical verification tool used to automatically enlarge small area shapes
    - Area for some cells had to be increased
    - All optimized cells characterized and delivered in a DFM library

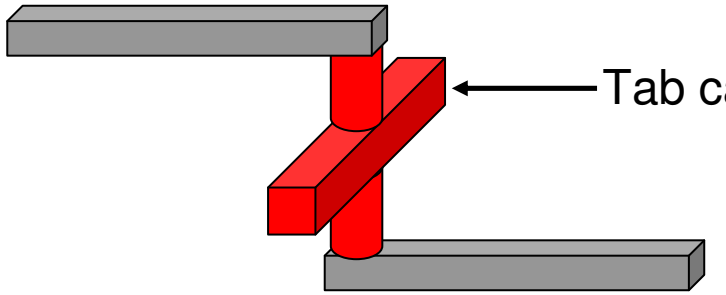


Before

After

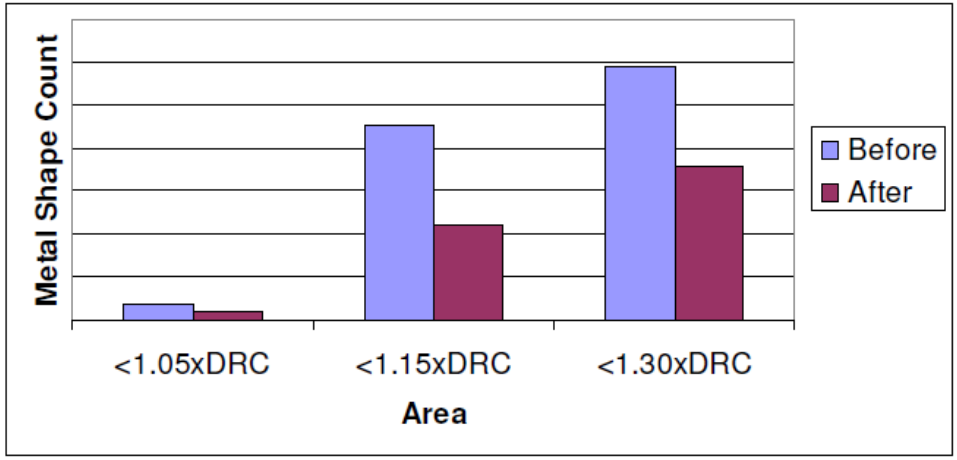
Block-Level Optimization

- ►Post-route flow to opportunistically use DFM cells
  - In routed design, swap in DFM cells in place of their non-DFM variants
  - Time, revert DFM cells with negative setup/hold slack
    - Works well in practice as DFM cells have negligibly different timing
  - ECO route, revert DFM cells to address design rule/connectivity violations
- ►Minimizing small area shapes in routing
  - Stacked vias used by router to skip layers. Stacked vias have small area tab.



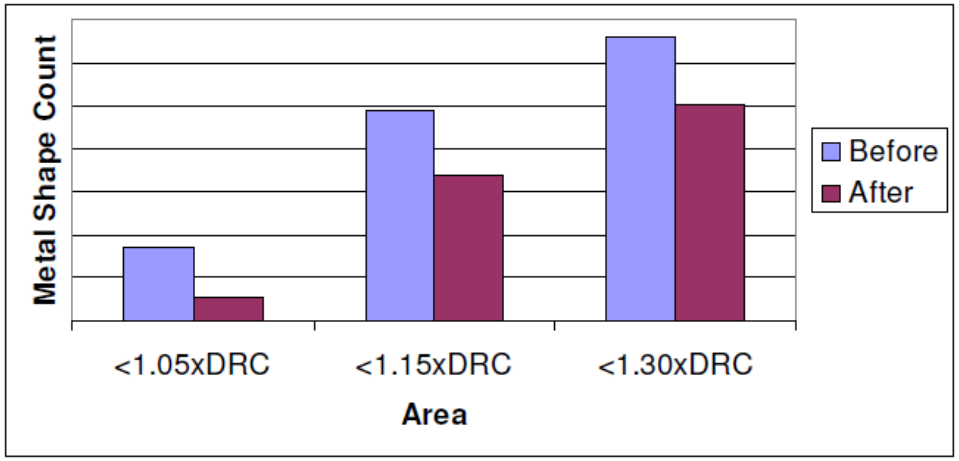
  - Add stacked vias to Technology LEF that have larger tabs
  - Preferentially use larger-tab stacked vias in routing
    - Functionality provided by the router
    - Reroute and ECO route flows used

Results



Metal 1

Reduction primarily due to DFM cells



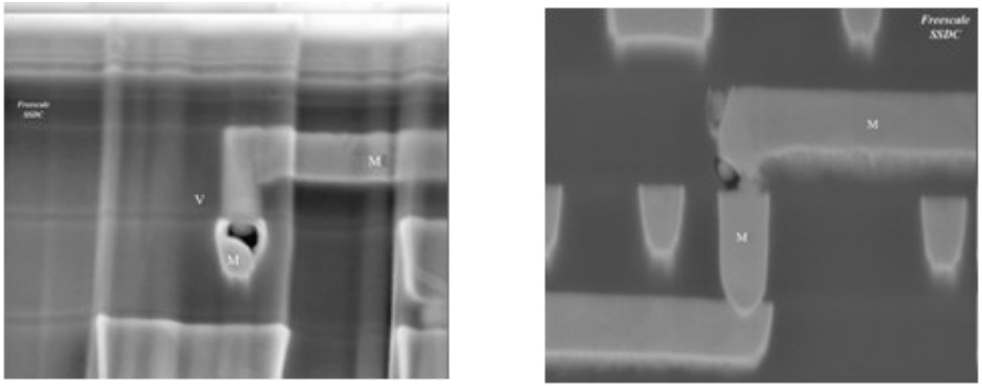
Metal 2

Reduction primarily due to use of larger-tab vias in routing

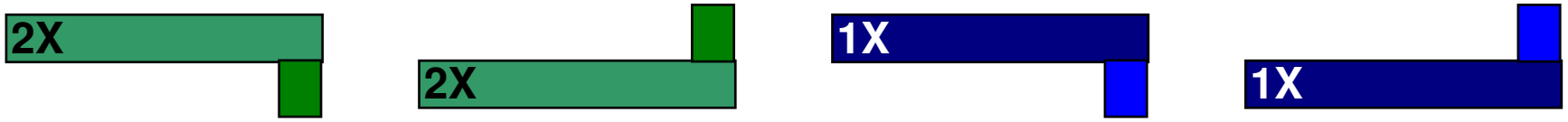
Metals 3 and above not significant contributors to small area metal

Via Voids at Line Ends (VVLE)

- VVLE due to well-known stress voiding mechanism
  - Voids at line ends migrate towards vias and cause open/high resistance
  - Particularly severe in one our advanced technologies → qualification delayed



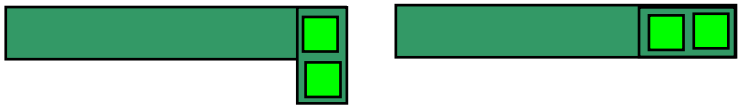
- Improvements in process and qualification inadequate
  → DFM fix needed (=minimize # VVLE-prone configurations)
- VVLE-prone configurations



Priority 1 **Priority 2** **Priority 3** **Priority 4**

Mitigating VVLE

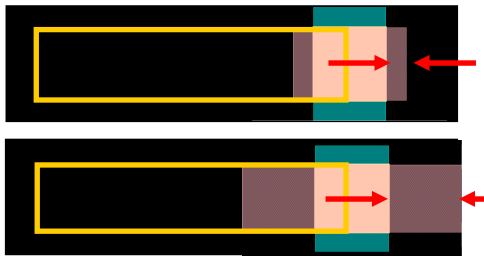
- Layout modifications deemed beneficial



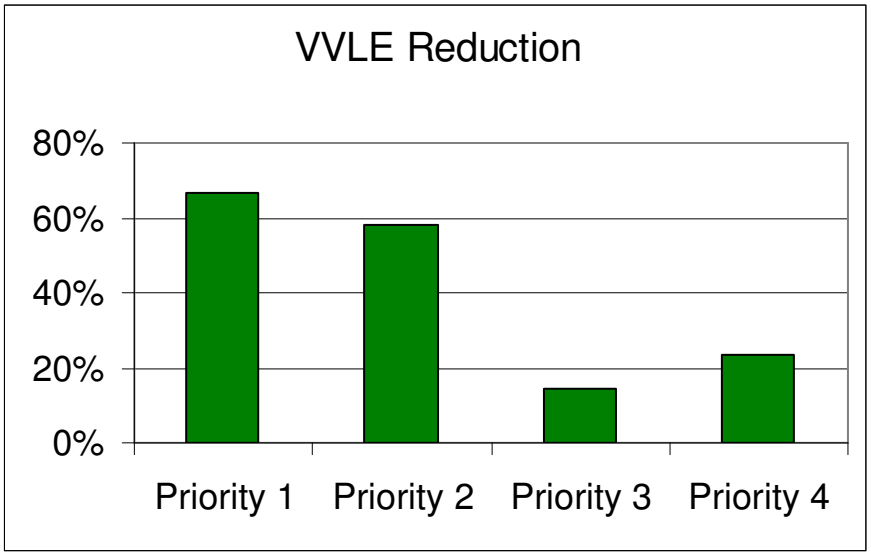
Via doubling

Increasing wire extension

- Via optimization flows already used
- Increasing wire extension
  - Add DFM via definitions with large extensions to Technology LEF

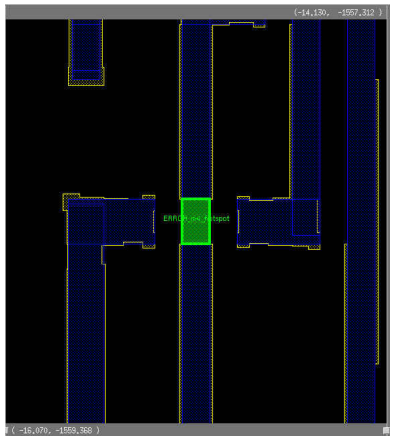


  - ECO and full routing flows developed to preferentially and opportunistically DFM vias

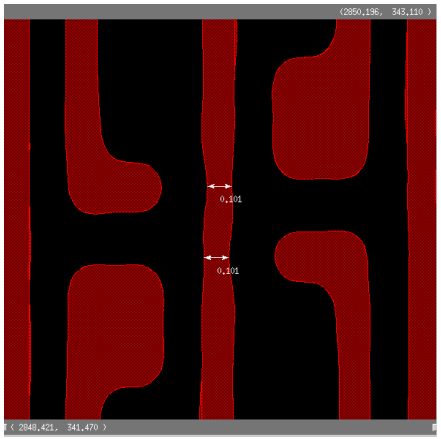


Late-Breaking Litho Hotspot

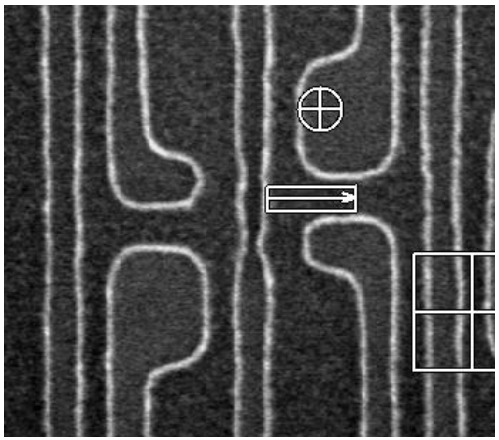
- ►Litho hotspot analysis and fixing are well-known DFM techniques
- ►Foundries supply litho hotspot kits
  - However, litho process constantly evolves so litho kits are out-of-date and inaccurate
  - Also, chip-level litho analysis is fast but inaccurate
- ►Litho hotspots determined to be a significant yield detractor



Exemplary config



Simulated image

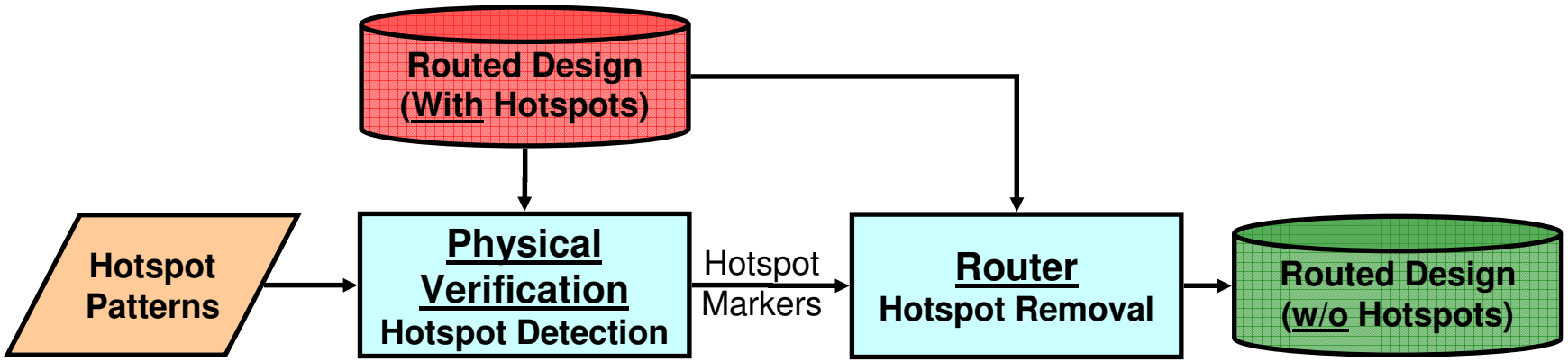


SEM (on Silicon)

- ►OPC ineffective. Process improvement too expensive!
  - → DFM solution needed to minimize hotspots

Removing Litho Hotspots

- Litho hotspot removal flow



- Results
  - Over two orders of magnitude reduction in number of hotspots. Typically, 100,00 to 100
  - Remaining hotspots fixed manually
- Flow consistently applied on all products → process improvement investment put on hold

Summary

- Design cycle begins much before process is mature and limitations are known
- Failure analysis is used to identify yield detractors especially on early test vehicles and products
- Yield detractors found in FA generally get resolved in process but it often quicker and cost-effective to develop DFM techniques to resolve in design
- FA-driven DFM techniques should be effective, quick developed and applied, cause minimal churn
- We presented three FA-driven DFM techniques to:
  - minimize number of small area metal shapes;
  - minimize number of layout configs susceptible to via voiding at line ends;
  - eliminate litho hotspots not caught by model-based litho hotspot detection.
- FA-driven DFM improves yield during process rampup and may reduced time to market.


freescale™
semiconductor