I. INTRODUCTION

Rambus is developing IP blocks at advanced process nodes. Silicon variability, inherent to 45nm process nodes and below, can impact both the physical integrity and the parametric performance of the design, so it is equally important to optimize the chip manufacturability along with the more traditional area, speed and power optimization. Our designers must implement a design methodology that also meets the foundry requirements for advanced process nodes. Beginning at 45nm, most foundries have made design-side lithography checks mandatory. Therefore it is critical for Rambus to integrate a multi-foundry litho analysis for both custom and automated place-and-route designs with a minimum disruption in the methodology and impact on design cycle time.

In this paper, we outline these challenges and requirements from the designer point of view. We also describe the litho analysis solutions that we have deployed with success at 40 nm and 28 nm. We explain the key criteria of this success and provide quantified runtime results as well.

II. LITHOGRAPHY ANALYSIS MOTIVATIONS

As technology migrates to the 45-nm node, fast yield ramp-up is increasingly difficult to achieve due to the sub-wavelength effects of lithography.

The industry has currently two different approaches to check lithography and identify hotspots on the design side. One is based on a model-based simulation that predicts the silicon image of the design shapes and detects where the fidelity between silicon and design intent is problematic, or where printability is too challenging, inducing too much variability. The other approach is based on a pre-defined set of yield-limiting patterns that must be identified and then removed from the design prior to manufacturing.

Model-based or pattern-based, the lithography analysis is part of mandatory foundry requirements, and fatal hotspots must be fixed prior to tape-out.

III. LITHOGRAPHY ANALYSIS CHALLENGES

When first introduced lithography analysis was done by the fab after optical proximity correction just prior to mask making. To avoid finding these defects on silicon, thorough model-based checks were done to identify and fix these “hotspots” prior to mask making. But as process technologies evolved, the number of hotspots increased and correction became more challenging because the degree of freedom is very limited at that late stage of the design. Foundries started to recommend at 65 nm and, at 45 nm and below have made it a mandatory step to identify and correct these hotspots on the design side during digital or custom implementation. Physical verification has been augmented with litho sign-off. It has been quite disruptive to find hotspots during tapeout, and equally hard to fix them. The need to create litho-clean layout during creation emerged and required a tighter integration of the litho checks in design implementation. In-Design litho analysis and fixing which consists of tight integration of the litho analysis into the implementation tools to detect the hotspots during design, along with automated correction to remove the hotspots has been a key contributor to the adoption of litho-aware designs. Since we design both custom and cell-based design flows at Rambus; integration into both Cadence Virtuoso and Encounter were key criteria for selecting a litho analysis tool.

Even with strong motivations and mandatory checks imposed by foundries, it is challenging to add new tasks to design flows. So it is important to implement a convergent, fast and integrated flow to get it accepted by designers.

Finally, Rambus IP can be targeted to multiple foundries using different lithography analysis approaches. So it was a key requirement that the tool selected to perform the mandatory lithography analysis can support both a model-based and a pattern-based approach, and that it has been qualified by our target foundries.

III. LITHO-AWARE CUSTOM LAYOUT

Some of our designs are done using a custom layout methodology. We create cells and blocks from scratch and we need to ensure that they meet the manufacturability requirements mandated by the foundries. We designed our custom layout in Cadence Virtuoso and we needed a litho analysis that met the requirements outlined in section II:

- Minimum overhead and ease of use for our custom designers
- Support multi-foundry requirements and support both model-based and pattern-based litho checks

First of all, Cadence Litho Physical Analyzer (LPA) supports both model-based and pattern based litho checks (see Figure 1) and has been certified by all
major foundries. Moreover, LPA has been integrated into Virtuoso so that designers can easily check litho manufacturability during custom layout, import hotspot found and then fix them using the suggested fixing guidelines generated by LPA (see Figure 2).

IV. LITHO-AWARE DIGITAL IMPLEMENTATION

Other IP blocks are implemented using a traditional synthesis and place-and-route methodology. In one of our 28nm design, the litho sign-off detected around 450 hotspots on the routing layers. We turned then on the litho-aware routing available in Cadence Encounter Digital Implementation System to reduce as much as possible the number of hotspots during routing. Litho prevention improves the routing quality but foundry-specific litho sign-off must still run on the layout to detect the remaining hotspots. The complexity of digital designs not only requires a tight integration to detect hotspots but also demands automated fixing. The facts that LPA is integrated into Encounter (see Figure 3) and that Encounter offers an automated fixing solution was a great asset to ease adoption by our digital designers. Once the hotspot detection has been done, the hotspot can be loaded into Encounter for automated fixing and then an incremental check is performed to make sure that the fixing did not introduce any new hotspot and that the design is litho clean.

The complete litho-aware flow applied on our 40 nm and 28 nm designs is shown in Figure 4. In the design mentioned above, we systematically activated the litho-prevention option and used LPA to run litho signoff, detect the remaining hotspots and Encounter fixed them all, delivering a 100% fixing rate. Our designs were litho clean at the end.

LPA supports both model-based and pattern-based methodologies. This enables to not only support multi foundries, but it is used to speed-up In-Design checks. During the implementation loop, model-based litho analysis is too computational intensive and LPA leverages its pattern-matching technology to identify where to run the model checks. This reduces dramatically the runtime as shown in table 1 and allows detecting and fixing most if not all hotspots during implementation. Having a quick turn-around time during implementation is critical for adoption.

When pattern-based analysis is the foundry litho sign-off, pattern-based analysis showed a tremendous runtime advantage. We typically saw LPA pattern-based checks to be several orders of magnitude faster than the model-based approach. This means that the litho check can be reduced from weeks to hours.

V. SUMMARY

For both custom and digital designs at 40 nm and 28 nm, we easily adopted LPA because of its multi-foundry support and also because of the ease of use due to seamless integration within Virtuoso and Encounter.

<table>
<thead>
<tr>
<th>Design</th>
<th>Size</th>
<th>Area</th>
<th># CPUS</th>
<th>Model-based Runtime</th>
<th>Pattern-based Runtime</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test case #1</td>
<td>3.94 GB</td>
<td>7200u X 4200u</td>
<td>32 CPU</td>
<td>17 hour 25 min</td>
<td>2 hour 10 min</td>
</tr>
<tr>
<td>Test case #2</td>
<td>1.40 GB</td>
<td>5300u X 2500u</td>
<td>16 CPU</td>
<td>9 hour 41 min</td>
<td>10 min</td>
</tr>
<tr>
<td>Test case #3</td>
<td>835 MB</td>
<td>3300u X 3000u</td>
<td>16 CPU</td>
<td>4 hour 23 min</td>
<td>7 min</td>
</tr>
</tbody>
</table>

Table 1: Litho Detection Runtime

Figure 1: Pattern-based litho check in Virtuoso

Figure 2: LPA hotspot and fixing guidelines
Figure 3: Litho Analysis in Encounter

Litho Prevention

Litho Analysis

Automated Litho Fixing

Incremental Litho Fixing

Figure 4: Encounter Litho-aware Flow